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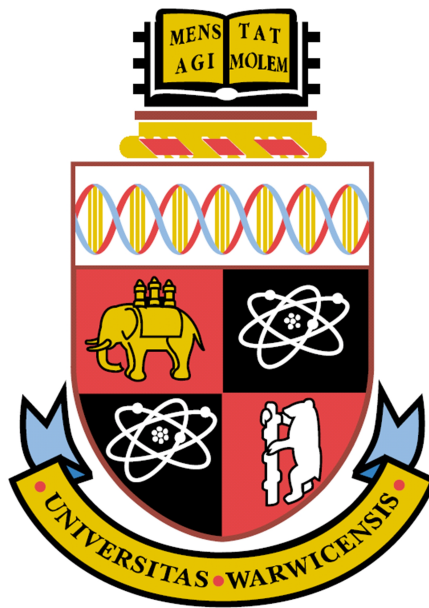
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# Utilising Power Devices Below 100 K to Achieve Ultra-low Power Losses



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Dissertation submitted for the degree of  
*Doctor of Philosophy*  
August 2011





# Declaration

The work presented in this thesis was carried out in the School of Engineering, University of Warwick, during the period October 2007 to August 2011 under the supervision of Prof. Philip Mawby.

The author wishes to declare that apart from commonly understood and accepted ideas, or where reference is made to the work of others, the work in this thesis is his own. It has not been submitted in part, or in whole, to any other university for a degree, diploma or other qualification.

K. K. Leong

August, 2011



*“To Kuan, for her TLC which I cannot live without, for her patience which I  
can never repay”*

*“To my loving parents, who provided me with the foundation to stand upon to  
reach for success”*



## Acknowledgements

Firstly, I would like to my supervisors Prof. Philip Mawby and Dr. Angus Bryant, for their guidance and support through out my PhD studies. I learned a great deal of knowledge and skills from them and I shall be forever grateful.

I would also like to thank Converteam UK for their initiation and financial support for this project. Their work is a beacon of light for the UK industry and I am proud to be associated with it. Special thanks to Dr. David Hinchley, Joseph Eugene and Martin Ingles for our numerous meetings and discussions.

I must thank my colleagues within the PEATER group, especially Benedict Donnellan for his numerous help with my work and our daily chat about random topics, Dr. Nii-Adotei Parker-Allotey for his aid when I hit a Latex wall, Dr. Shaoyong Yang for his knowledge on the topic, Dr. C.F. Tong for his overall helpfulness and useful advices, Dr. James Covington for lending the chiller to me and never remembered to ask for it back and Dr. William (Bill) Croft for his support over the years. I would also like to thank Stewart Edris and his fellow technicians for their helpful advices and excellent workmanship. I must also thank Tim Naylor from the Physics department for his help and advices for the cryogenic system.

Finally, I would like to thank all my friends and colleagues within the University of Warwick, whom I have not mentioned but deserved my thanks nevertheless. Thank you.



# Abstract

One of the main trend in the development of high power electric machines (motors, generators) is to replace the magnetic components with superconducting wires, this inevitably leads to a critical requirement from the industry (Converteam) to operate power devices at cryogenic temperatures. However, the current understanding of the behaviour power devices at cryogenic temperatures is limited, especially below the liquid nitrogen temperature of 77 K. This is a problem since most of the superconducting wires operate at temperatures below 77 K. Furthermore, it is uncertain which device type is better, if at all suited to cryogenic operation. In order to answer this, a thorough analysis of the known cryogenic behaviour of all the generic power devices was performed, including the physical behaviour of silicon at cryogenic temperatures. It is concluded that the power MOSFET is the best likely candidate for cryogenic operation.

To understand the cryogenic behaviour of silicon power MOSFETs especially between the temperatures of 20 K and 100 K, a cryogenic measurement system was built to characterise different types of power MOSFETs. All the measured power MOSFETs exhibited large improvement in on-state resistance down to 50 K and non-linear degradation of breakdown voltages with lower temperatures. Various behaviour was observed below 50 K including carrier freeze-out, electric field dependent ionisation of free charge carriers and large variations in on-state resistance between identical devices. Several power Schottky diodes were also characterised and all exhibited merged PiN Schottky diode behaviour at cryogenic temperatures. Non-silicon devices such as silicon carbide power MOSFETs and gallium nitride HEMTs were also measured. Silicon carbide exhibited no improvements at cryogenic temperatures, whereas gallium nitride HEMTs may prove to be the best power device to be utilised in future cryogenic applications.

Since unusual behaviour was observed in power MOSFETs below 50 K, an attempt was made to explain these phenomena using theoretical equations of semiconductor physics and analytical models of power MOSFETs. The author suggested that careful control of the dopant concentration at the accumulation region below the oxide gate is required to improve the power MOSFET operations below 50 K. Moreover, the super-junction power MOSFETs could be optimised for better cryogenic operation.

It is the intention of this work to demonstrate the benefits of power MOSFET cryogenic operation in a realistic industrial application. A demonstration model was designed and simulated, this circuit uses a back-to-back power MOSFETs configuration to control the free-wheeling current flowing through a high temperature superconducting coil. The electrical and thermal design of the model has been described, simulated and presented in this work.





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# Nomenclature

<i>Al</i>	Aluminium
<i>As</i>	Arsenic
<i>B</i>	Boron
<i>GaAs</i>	Gallium Arsenide
<i>GaN</i>	Gallium Nitride
<i>Ge</i>	Germanium
<i>MPS</i>	Merged PiN/Schottky
<i>P</i>	Phosphorus
<i>Si</i>	Silicon
<i>SiC</i>	Silicon Carbide
<i>SiGe</i>	Silicon-germanium
<i>SiO<sub>2</sub></i>	Silicon dioxide
<i>SIPMOS</i>	Siemens Power Metal Oxide Semiconductor
<i>TMBS</i>	Trench MOS barrier Schottky
2D	Two dimensional
AlGaN/GaN	Aluminium gallium nitride/gallium nitride hetero-junction
AMLE	Advanced Magnet Lab Energy
AMSC	American Superconductor Corp.
ASG	Adjustable speed generators
BSCCO	Bismuth strontium calcium copper oxide
CMOS	Complementary metal-oxide-semiconductor
DC	Direct current
EPC	Efficient power conversion
EST	Emitter switched thyristor
FCT	Field controlled thyristor
FETs	Field effect transistors
GE	General Electric
GTO	Gate turn off
HBT	Heterojunction bipolar transistor
HEMT	High electron mobility transistor
HFET	Hetero-junction field effect transistor
HTS	High temperature superconducting

ICASE	Industrial Co-operative Awards in Science and Engineering
IGBT	Insulated-gate bipolar transistor
IV	Current-voltage
JFET	Junction field effect transistor
JV	Current density-voltage
LEDs	Light-emitting diodes
LHC	Large hadron collider
MCT	MOS controlled thyristor
MESFETs	Metal semiconductor field effect transistors
MISFETs	Metal-insulator-semiconductor-field-effect-transistors
MODFET	Modulation-doped field effect transistor
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide semiconductor field effect transistor
MRI	Magnetic resonance imaging
NASA	National Aeronautics and Space Administration
NBG	Narrow band-gap
NPT	Non-punch-through
OFHC	Oxide-Free High Conductivity
PCB	Printed circuit board
PID	Proportional-integral-derivative
PiN	P-type - intrinsic - N-type (diode structure/behaviour)
PLECS	Piecewise linear electrical circuit simulation
PT	Punch-through
RF	Radio Frequency
SCR	Silicon controlled rectifier
SITh	Static induction thyristor
SJ	Super-junction
TRIAC	Triode for alternating current
VDMOS	Vertical diffused metal-oxide-semiconductor
VLSI	Very-large-scale integration
WBG	Wide band-gap
YBCO	Yttrium barium copper oxide

$\alpha_{eff}$	Effective ionisation rate ( $cm^{-1}$ )
$\alpha_n$	Electron ionisation rate ( $cm^{-1}$ )
$\alpha_p$	Hole ionisation rate ( $cm^{-1}$ )
$\beta$	Common base current gain for power BJT
$\mathbb{E}$	Electric field ( $V/cm$ )
$\mathbb{E}_c$	Critical electric field ( $V/cm$ )
$\mu_{FE}$	Field effect electron mobility ( $cm^2/Vs$ )
$\mu_n$	Electron mobility ( $cm^2/Vs$ )
$\mu_p$	Hole mobility ( $cm^2/Vs$ )
$\phi_{bn}$	Schottky barrier height ( $eV$ )

$\rho$	Resistivity ( $\Omega cm$ )
$\sigma$	Conductivity ( $S/cm$ )
$\tau$	Excess carrier lifetime(s)
$\tau_n$	Electron lifetime (s)
$\tau_p$	Hole lifetime (s)
$\varepsilon_0$	Permittivity in vacuum $8.85 \times 10^{-14}$ ( $F/cm$ )
$\varepsilon_{si}$	Dielectric constant of silicon 11.68
$\varepsilon_s$	Permittivity of silicon $1.0337^{-12}$ ( $F/cm$ )
$^{\circ}C$	Celsius
$A^*$	Effective Richardson constant, for n-type silicon 110 ( $A/cm^2/K^2$ )
$E_0$	Energy band gap at 0 K (eV)
$E_C$	Bottom of the conduction band edge (eV)
$E_D$	Donor energy level (eV)
$E_g$	Energy band gap (eV)
$E_i$	Ionisation energy (eV)
$E_V$	Top of valence band edge (eV)
$HK$	Surface micro-hardness ( $kg/mm^2$ )
$I_B$	Base current for power BJT (A)
$I_{CEL}$	Collector-emitter leakage current for power BJT (A)
$I_C$	Collector current for power BJT (A)
$I_F$	Forward current (A)
$I_{Gth}$	Gate threshold current, (A)
$J_F$	Forward current density( $A/cm^2$ )
$J_S$	Saturation current density ( $A/cm^2$ )
$K$	Thermal conductivity ( $W/Kcm$ )
$k_B$	Boltzmann constant $\simeq 1.38 \times 10^{-23}$ ( $cm^{-3}$ )
$L_n$	Electron diffusion length ( $cm$ )
$L_p$	Hole diffusion length ( $cm$ )
$m_0$	Electron rest mass $\simeq 9.11 \times 10^{-31}$ (kg)
$m_n^*$	Effective mass of electron (kg)
$m_p^*$	Effective mass of hole (kg)
$n$	Electron density ( $cm^{-3}$ )
$N_A$	Acceptor concentration ( $cm^{-3}$ )
$N_C$	Effective density of state for conduction band ( $cm^{-3}$ )
$N_{drift}$	Dopant concentration of the drift region ( $cm^{-3}$ )
$N_D$	Donor concentration ( $cm^{-3}$ )
$n_i$	Intrinsic carrier concentration ( $cm^{-3}$ )
$N_V$	Effective density of state for valence band ( $cm^{-3}$ )
$p$	Hole density ( $cm^{-3}$ )
$q$	Electron charge $\simeq 1.60 \times 10^{-19}$ (C)
$R_{accu}$	Resistance of the accumulation layer ( $\Omega$ )
$R_{chan}$	Resistance of the channel ( $\Omega$ )
$R_{drift}$	Drift layer resistance ( $\Omega$ )
$R_{JFET}$	Resistance of the JFET region ( $\Omega$ )



$R_{sub}$	Substrate resistance ( $\Omega$ )
$R_S$	Series resistance ( $\Omega$ )
$T$	Temperature (K)
$T_C$	Superconducting transition temperature (K)
$V_{BD}$	Breakdown voltage (V)
$V_{BD}(300)$	Breakdown voltage at 300 K (V)
$V_d$	Voltage drop across drift region (V)
$v_d$	Drift velocity ( $cm/s$ )
$V_F$	Forward voltage (V)
$V_{GS}$	Gate source voltage (V)
$V_{Gth}$	Threshold voltage of the gate (V)
$V_J$	Voltage drop across the PN junction (V)
$v_{sat}$	Saturation velocity ( $cm/s$ )
$V_{Sch}$	Voltage drop across the Schottky barrier (V)
$W_{Dm}$	Depletion width (cm)
$W_d$	Drift region thickness ( $cm$ )
$W_t$	Drift region thickness ( $cm$ )
CTE	Coefficient of thermal expansion ( $10^{-6}/K$ )
K	Kelvin



## 1.1 Background

We, as a global society are heading towards a major energy crisis. Our dependence on fossil fuel will soon reduce world reserves to exigency levels. Assuming current consumption, oil will run out in 45 years and natural gas stocks will be depleted in 64 years [1]. As reserves reduce, prices will rise and the knock on effects will become far too clear in our society. Alternatives, such as nuclear power, are controversial and not without risk. Nuclear fuel used to generate electricity can be further enriched to make nuclear weapons, nuclear stations are vulnerable from attacks and natural disasters. Also, nuclear waste can take thousands of years to decay to safe levels. On the whole, it is unwise to use nuclear power as the long term solution for our energy crisis. In recent years, renewable energy has become the leading topic in business, research, social awareness and politics. Most energy related companies have redirected much of their business into the renewable energy sector, this has pushed both commercial and academic research to advance at an incredible pace. The general public awareness has also been slowly increasing and acceptance of renewable energy technologies has been generally favorable [2]. Most of the world's major governments have acknowledged the upcoming energy crisis and have promised to set major targets to integrate various renewable energy technologies into their existing power infrastructure. The United

Kingdom has set a target of sourcing 15 % of its total energy from renewable sources by 2020 [3]. This can be achieved by a combination of on-shore and off-shore wind power, hydroelectricity, as well as wave and tidal energy. Furthermore, wind power (especially offshore wind) has been highlighted as the leading technology and is projected to have the biggest growth of all technologies in the coming years as stated in a quote from the UK renewable energy strategy 2009 below.

*“Wind power is currently one of the most developed and cost-effective renewable electricity technologies. The UK has the largest potential wind energy resource in Europe. While offshore wind is more technologically challenging and more expensive than onshore wind, it has a larger potential due to a stronger and more consistent wind resource out to sea, leading to higher power outputs per turbine and more hours spent generating each year.”*

The UK Renewable Energy Strategy 2009 [3].

### 1.1.1 Development of Wind Turbine Technology

A wind turbine is a generic name given to any wind power system that converts wind energy into various forms of energy. This could be mechanical energy to operate water pumps in rural areas or electrical energy for the national grid. The first electricity generating wind turbine was installed in Denmark in 1891. However, wind turbine development has been relatively slow through the last century due to the dominance of high energy density fossil fuels as the main energy source for power generation.

Although wind turbines can come in all shapes and sizes, the most commonly adopted design is the three bladed rotor, horizontal axis turbine, placed on top of a high tower. For electrical applications, the wind turbine has a nacelle which houses the gear box and generator, connected to a transformer on the ground that feeds straight to the grid. Fig. 1.1 presents the basic components of a wind turbine, from the rotor to the grid.

There are numerous concepts for the electrical design of wind turbines. These include the basic Danish concept of constant speed and fixed-ratio gearbox; the dynamic and cost effective adjustable speed generators (ASG); more advanced ASG concepts such as doubly

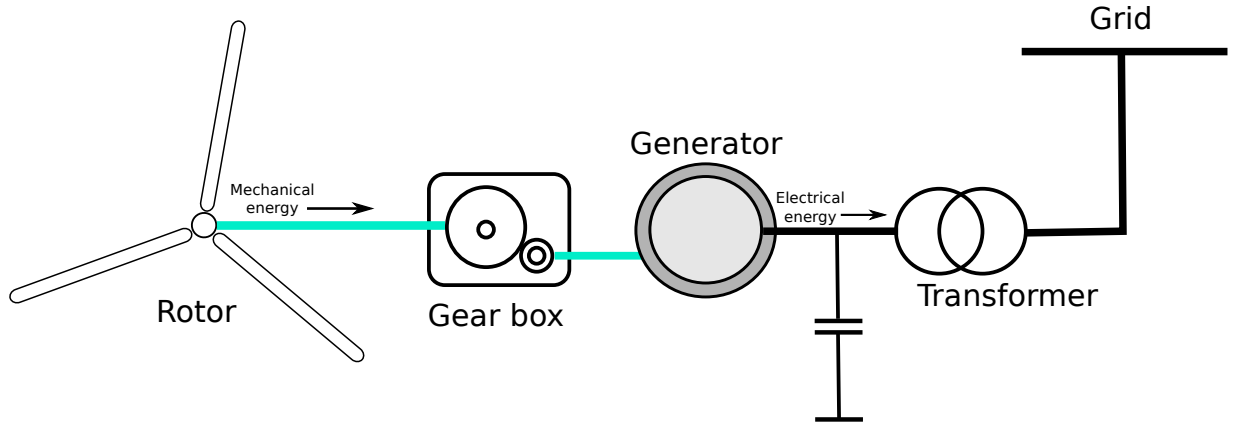


Figure 1.1: The basic components in a wind turbine.

fed induction systems, etc. However, all these concepts involve the use of a gearbox which has proven in the past to have reliability problems [4], this becomes particularly costly in offshore applications [5]. Therefore, gearbox-less concepts such as direct drive permanent magnet generators are becoming more attractive, especially at high power ratings. The result is a large rotor, low speed, high torque system. The direct drive system improves mechanical reliability and robustness, has lower maintenance costs and increased efficiency, and a simplified nacelle design. However, direct drive generators are large compared to other design concepts. In order to increase the power ratings, the rotor must be even bigger and there is a physical and production limit on how big the rotors can get. Furthermore, permanent magnets require a high density of neodymium-based rare earth materials which are costly to source.

The most advanced concept in wind turbine design is the high temperature superconducting (HTS) generator. In this technology, HTS wires replace the permanent magnet component seen in direct drive systems. Superconductivity occurs in certain materials below a superconducting transition temperature ( $T_C$ ), where the electrical resistance is effectively zero and in theory an electric current can flow in a loop indefinitely without a power source. HTS wires are made from materials that have a ( $T_C$ ) above 30 K ( $-243.2^\circ\text{C}$ ). HTS technologies have already found uses in motor applications such as marine propulsion systems and therefore have a relatively high level of maturity. Fig. 1.2 shows the improvement in

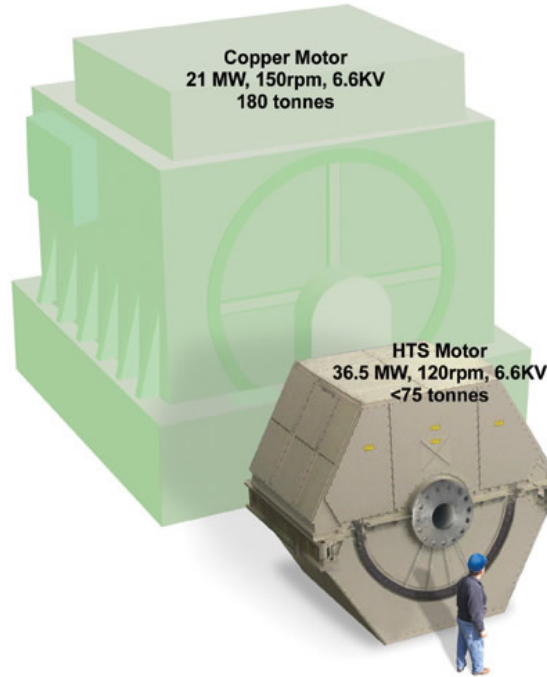


Figure 1.2: Illustration to show size difference and increased power output from a HTS 36.5 MW ship propulsion motor, compared to a conventional system [6].

size and power for ship propulsion motor with and without HTS technology [6]. Due to the high current density that can be achieved in HTS coils, the power density can increase beyond that of a permanent magnet system of the same size. The overall efficiency of the whole system also improves. HTS technologies can also reduce the overall size and weight of the generator, which is extremely advantageous in reducing the cost of the wind turbine structure. The size of the nacelle can be reduced, the structure of the tower can be simplified as can the foundation support. Several major companies have already been working on the HTS concept: American Superconductor Corp (AMSC) and Advanced Magnet Lab Energy (AMLE) have been working on 10 MW wind turbine direct drive HTS generator systems; Converteam and Zenergy Power have been working together to develop an 8 MW direct drive wind turbine based on Zenergy's HTS coils. Fig. 1.3 presents the schematics of the small generator within the nacelle [7]. The same team has already produced the world's first HTS hydroelectricity generator to be installed in Germany [8].

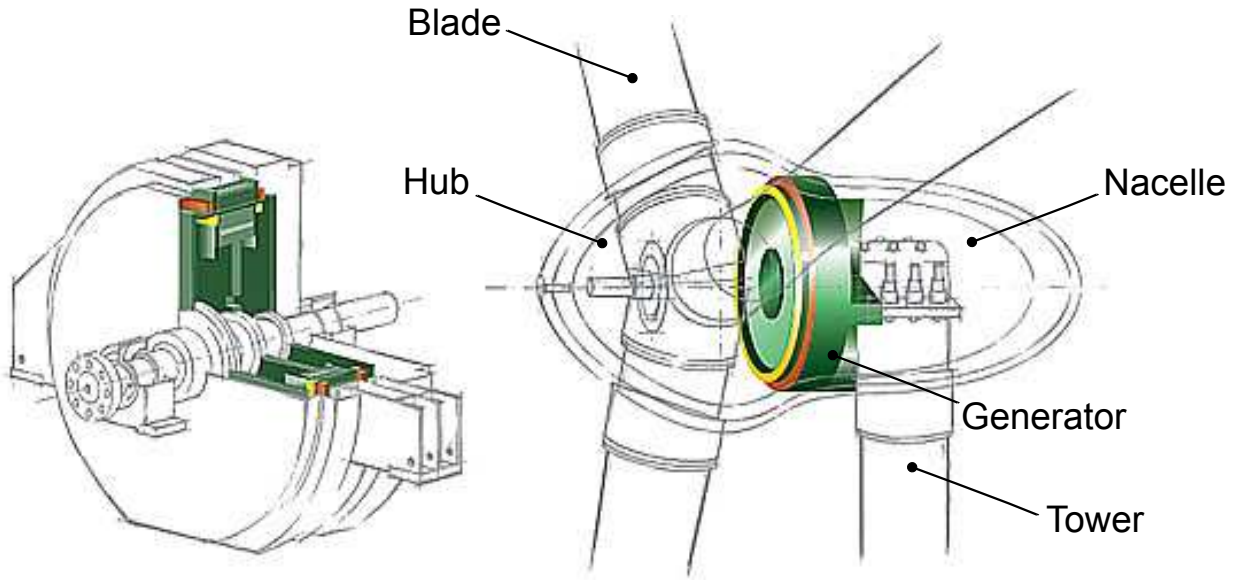


Figure 1.3: Schematics of small 8 MW direct drive HTS generator for wind turbine [7].

### 1.1.2 The Important Role of Power Electronics

The role of power electronics is to control the flow of electrical energy within power systems. This can be to condition the voltage, current, frequency or phase to the required state for the load. This is essential in electrical energy generation, transportation and consumption. Power electronics can be found in virtually all electrical appliances from radios, mobile phones, TV, personal computers to industrial motors, power stations and wind turbines. It can be said that power electronics have been the silent work horse that drives our modern society, without it our society as we know it will cease to function and yet most of the general public have no awareness of their existence or importance.

With the cost of energy and the demand for high power density systems increasing in the past decades, there has been an universal trend to improve the efficiency of power systems. This has lead to a steady growth in power electronic technologies. Mainly in the advancement of power semiconductor devices so that they can handle higher power and operate more efficiently. The major land mark developments for power electronic switches are the thyristors and the gate turn off thyristors (GTO) in the high voltage range. The insulated-gate bipolar transistor (IGBT) for the medium voltage range and the power metal-

oxide semiconductor field effect transistor (MOSFET) for the low to medium voltage range. For power diode development, there are the p-type intrinsic n-type (P-i-N) diode for high voltage, high power applications and Schottky diode for high speed, low power applications.

Silicon has been the dominant semiconductor material for the power electronics industry. This is due to its mature fabrication processes, which has been inherited from the development of technologies such as very-large-scale integration (VLSI). However, power electronic developers have been looking to other semiconductor materials that have superiority properties when compared to silicon, such as silicon carbide ( $SiC$ ) and Gallium Nitride ( $GaN$ ). These can exhibit lower conduction loss, higher breakdown voltages, wider operational temperature range, higher switching frequency, higher power handling capability and higher reliability.

## 1.2 Motivation

As an industry funded academic research, the aim of this work has been driven entirely by industrial requirements. The project is an *industrial co-operative awards in science and engineering* (ICASE) [9] award in collaboration with Converteam UK, as the industrial partner [10]. As previously discussed, the Converteam UK advance technology group has been working on HTS direct drive wind turbine systems. One of the main problem with their existing design is the high thermal leakage of the electrical interconnects from the warm regions into the cold regions. In order to address this problem, Converteam has filed a patent (GB2423652) for a free-wheeling *exciter assembly*, designed to supply current to the rotor winding of a HTS synchronous machine [11]. Fig. 1.4 presents the exciter circuit topology. The circuit is split into warm stationary parts, warm rotating parts and cryogenic rotating parts. The idea here is to charge the HTS coil (16) with the warm stationary and rotating circuits and have a reverse-blocking gate-controlled semiconductor device (15) to provide the free-wheeling path for the field current. By placing the semiconductor device within the cryogenic environment, the electrical connections (14) to the warm part of the circuit can be minimised. This results in a reduction in the thermal leakage and cooling



requirements of the system. The aim is to free-wheel the field current between the HTS coil and the semiconductor device with relatively little current degradation, the current can be “topped up” with short voltage pulses between long intervals to sustain the required current level. The exciter assembly can be operated in four modes. The first is the “start up” mode where the field current is ramped up to the required level. The second is the “free-wheeling” mode where the current free-wheels indefinitely through the power device and HTS coil. The third is the “top up” mode where the field current is topped up by a short voltage pulse. The final mode is the “protection” mode during quench events in the HTS coils. A quench event is when part of the HTS coil loses its superconducting state and reverts back to a normal resistive state. The quenched part of the coil generates heat and rapidly raises the temperature of the surrounding regions which will cause quenched regions to spread. If the energy stored in the coil is not properly discharged, it could lead to irreversible damage to the HTS coil. A number of factors can lead to a quench event, these include excessive current, thermal leakage and defective material.

The HTS coil material can be made of bismuth strontium calcium copper oxide (BSCCO-2223,  $Bi_{2x}Pb_xSr_2Ca_2Cu_2O_{10}$ ) or yttrium barium copper oxide (YBCO,  $YBa_2Cu_3O_{7-\delta}$ ). These materials require operating temperatures below 110 K and 92 K respectively. For electric machine applications, they typically operate at less than 40 K. In this case, the expected operating temperature is between 30 K and 40 K.

Knowledge on the behaviour of power devices at such cryogenic temperatures is very limited. The main aim of this work is to investigate the feasibility of operating commercially available power electronic devices under those cryogenic conditions and identifying the best device for this application. The power device has the following requirements:

- The device has to be switchable between conducting and blocking modes.
- The device has to operate down to 30 K.
- The device has to achieve very low on-state resistance and power loss.
- The device has to be able to block sufficient voltages.

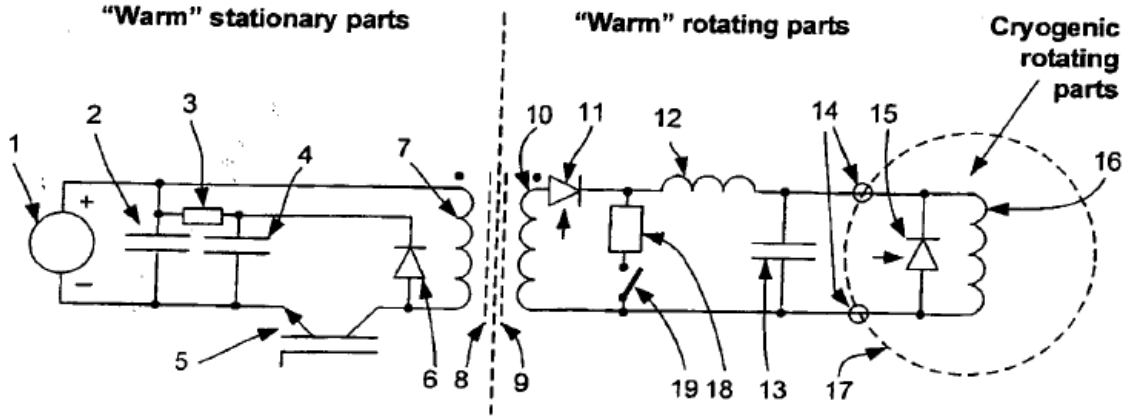


Figure 1.4: HTS Exciter circuit topology, the main parts are: 1 - DC power supply, 14 - electrical interconnects between warm and cold regions, 15 - freewheeling rectifying power device, 16 - HTS coil, 17 - cryogenic region, 18 - shunt resistor, 19 - shunt switch [11].

The investigation will be particularly focused on the temperature dependence of the forward voltage drops and breakdown voltages of various power devices. It is also the aim to physically demonstrate the free-wheeling action between the HTS coil and the suitable power device at 30 K.

## 1.3 Overview of thesis

The second chapter begins by introducing the various silicon based commercially available power devices and presenting their known cryogenic behaviour. The presented data was analysed and resulted in the conclusion that the power MOSFET is the best candidate power device for the intended application. The chapter will also introduce semiconductor materials beyond silicon and their devices' known behaviour at cryogenic temperatures. The last section briefly touches on the known reliability issues on power devices at cryogenic temperatures.

The third chapter introduces the known semiconductor (silicon) physics from room down to cryogenic temperatures. It focuses on the various parameters that affect the conductivity, such as the free charge carrier concentration and electron and hole mobilities. It also

introduces the breakdown mechanism and how it behaves at cryogenic temperatures.

The fourth chapter introduces the cryogenic system used in this investigation. As well as the explaining the different measurement systems used to characterise the power devices in the fifth chapter.

The fifth chapter presents the measured cryogenic behaviour of the various power devices. It mainly focuses on the different silicon based power MOSFET devices. This include conventional power MOSFET structures, p-channel power MOSFETs, high voltage power MOSFETs and various super-junction (SJ) MOSFETs. The measured cryogenic behaviour of a silicon carbide power MOSFET and a GaN HEMT are also be presented, as well as various forms of power Schottky diodes.

The sixth chapter analyses the presented data in chapter five through known equations and physical models in order to attempt to explain the observed behaviour in the power MOSFETs, as well as optimisation of power MOSFETs for operation below 50 K.

The seventh chapter presents the electrical and thermal design of the free-wheeling demonstration model.

The eighth chapter discussed concludes the thesis and discuss further work.

# An Introduction to Power Electronic Devices and their Behaviour at Cryogenic Temperatures

Silicon ( $Si$ ) is one of the most abundant elements on earth, it can be easily found in the Earth's crust in the form of common sand. Si is also the dominant material used in the semiconductor industry. No other semiconductor material contributes more than a tiny fraction to the number of commercially available devices. This also applies to the power device industry, where almost all devices on the commercial market are Si based. This stems from the fact that Si research has had decades in which to perfect the purification and growth process of Si crystals, therefore it is relatively easy and cheap to grow high purity large diameter Si wafers compared to other semiconductor materials. Si also has the advantage of having a high quality native oxide - silicon dioxide ( $SiO_2$ ), which is essential in metal-oxide-semiconductor ( $MOS$ ) based devices.

The core aim of this study is to find the power device that is both commercially available and most optimised for cryogenic operations. This is defined as the device that has the current-voltage (IV) characteristics that are closest to the ideal device behaviour. The ideal device behaviour has zero resistance during on-state with no voltage drop across the device and infinite reverse voltage capability in the off state. Such a device is unlikely to be realised, however it has been the target for device engineers to create a device which behaves as close to the ideal behaviour as possible. This chapter will introduce the various forms of Si power devices and their known behaviour at cryogenic temperatures. All the presented cryogenic

behaviour in this chapter has been measured by other authors and their data accurately extracted from their cited literatures.

## 2.1 Introduction to Silicon Power Devices and Cryogenic Behaviour

At present, commercially available power devices are not specifically designed for operation at cryogenic temperatures. Si based power devices are generally designed to operate in the range between  $-40\text{ }^{\circ}\text{C}$  and  $+150\text{ }^{\circ}\text{C}$  (some specify down to  $-55\text{ }^{\circ}\text{C}$  and up to  $+175\text{ }^{\circ}\text{C}$ ). Manufacturers do not guarantee device operation at lower temperatures because there has been insufficient demand for devices which operate at such extreme temperatures. Nevertheless, academic and commercial interests have measured the cryogenic behaviour of some common power devices, most of which will be presented in this chapter. The list of power devices has been split into power diodes (two-terminal devices) and unipolar and bipolar transistors (three-terminal devices). This will enable easy comparison of the cryogenic behaviour between two-terminal devices and highlight the major differences between unipolar and bipolar devices.

Unipolar devices also known as majority carrier devices, use only one type of charge carrier to conduct electricity. For n-type Si, the charge carriers are electrons; for p-type Si, the charge carriers are holes (further discussions into n and p-type Si will be presented in Chapter 3.1). Unipolar devices mainly conduct electricity via drift current (electric field driven). Bipolar devices also known as minority carrier devices, use both types of charge carriers simultaneously and conduct electricity via both drift and diffusion currents (driven by change in carrier density).

### 2.1.1 Power Diodes

Power diodes are two-terminal devices that can conduct in one direction whilst blocking current flow in the opposite direction. The generic IV characteristics of a power diode are

presented in Fig. 2.1. In the on-state, the voltage across the terminals has to be greater than the forward junction voltage before the device will turn-on. In the off-state, the device can only sustain a reverse voltage lower than the rated breakdown voltage before the device will begin to conduct in the opposite direction. In the past, power diodes tended to refer to PiN diodes as they were the only power diodes available that could be used in high voltage circuits. However, the development of high voltage Schottky diodes has lead to an additional choice for power diodes up to 300 V. Even more recent developments into trench MOS barrier Schottky (*TMBS*) diodes and merged PiN/Schottky (*MPS*) diodes has created new types of hybrid diodes that improve some of the shortcomings of the PiN and power Schottky diode designs.

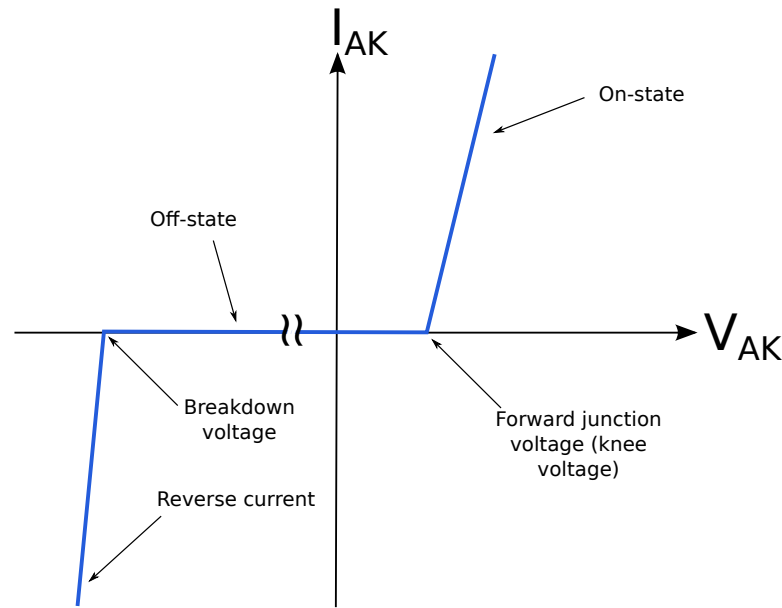


Figure 2.1: The general IV characteristic of a power diode.

### 2.1.1.1 Power Schottky Diodes

Schottky diodes are one of the most basic semiconductor devices. They consist of a metal layer in contact with a semiconductor material and can be considered as a unipolar device. The difference in the work function between the metal and the semiconductor in the metal-semiconductor junction creates a potential barrier, and effectively forms a rectifier. The

Schottky barrier height depends on the specific type of metal and semiconductor and it can be engineered to a wide range of values. The Schottky barrier height affects the forward voltage of the device as well as the reverse leakage current. The major benefits of Schottky diodes are high speed switching and a lower forward voltage drop compared to other power diodes.

As a power device, a Schottky diode has a lightly doped layer between the metal and the semiconductor substrate known as the drift region. This layer sustains the high reverse blocking voltage and is a common feature of power semiconductor devices. The main disadvantages of power Schottky diodes are that they have a high reverse leakage current and limited breakdown voltages. Most modern power Schottky diodes also employ P+ guard rings which aid the growth and shape of the depletion regions. This improves the breakdown capability of power Schottky diodes considerably. A typical vertical power Schottky diode structure is shown in Fig. 2.2(a). Fig. 2.2(b) shows the equivalent circuit diagram of the device. With the extra drift layer, the forward voltage ( $V_F$ ) is higher than a normal Schottky diode and can be expressed as the sum of all the series resistance:

$$V_F = V_{Sch} + I_F R_{drift} + I_F R_{sub} \quad (2.1)$$

$V_{Sch}$  is the voltage drop across the the Schottky junction,  $I_F$  is the forward current,  $R_{drift}$  and  $R_{sub}$  are the drift layer and substrate resistance respectively.

Previous research on the cryogenic behaviour of Schottky diodes has mainly focused on the inhomogeneity of the Schottky barrier which is emphasised at cryogenic temperatures [12], as well as simulation work from [13, 14]. Although most of the measured diodes are not actual power Schottky diodes, the Schottky barrier physics remains the same. The temperature dependence of the voltage across the Schottky junction can be approximated as [15]:

$$V_{sch} \approx \frac{kT}{q} \ln \left( \frac{J_F}{J_S} \right), \quad (2.2)$$

where  $J_S$  is the saturation current of the Schottky barrier and is related to the Schottky

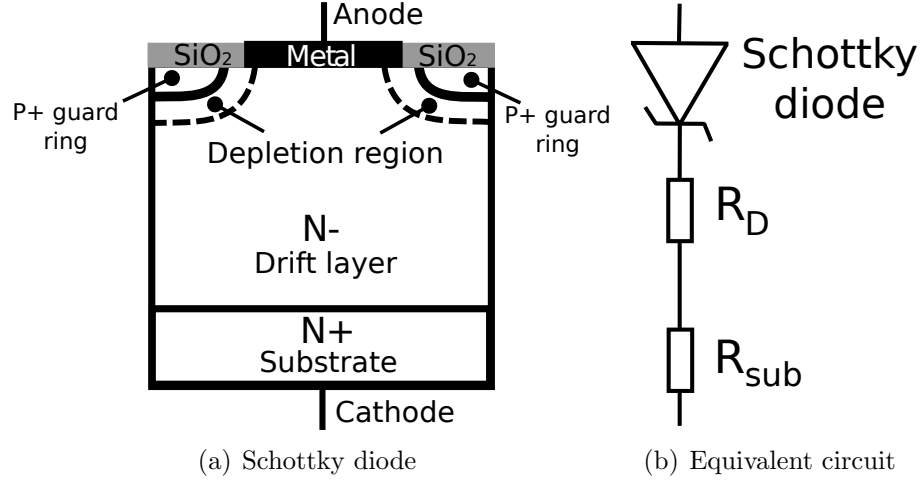


Figure 2.2: (a) The typical structure of a n-type power Schottky diode with P+ guard rings with  $SiO_2$  as isolation, the N- illustrate the lower doped drift layer and N+ as the highly doped substrate and (b) the equivalent circuit of the power Schottky diode with the series resistances.

barrier height ( $\phi_{bn}$ ):

$$J_S = A^* T^2 \exp - \left( \frac{q\phi_{bn}}{kT} \right). \quad (2.3)$$

$k$  is the Boltzmann constant,  $T$  is temperature,  $q$  is the charge of an electron,  $J_F$  is the forward current density and  $A^*$  is the effective Richardson constant (generally given as  $110 \text{ A/cm}^2/\text{K}^2$  for n-type Si). The cryogenic forward current density-voltage (JV) characteristics of a Schottky diode BYS 26-45 (Siemens, rated at 45 V, 3 A) has been measured by Simeonov and Kafedjiiska [12], the results are presented in Fig. 2.3. The forward voltage was found to increase as temperature decreases. The voltage required to reach  $1 \text{ A/cm}^2$  rises from  $\sim 0.3 \text{ V}$  at 294 K to  $\sim 0.6 \text{ V}$  at 82 K.

During reverse bias, a depletion region is formed that spreads from the metal/Si surface (where the peak field is located) into the drift region. A small leakage current flows through the device until the reverse bias reaches the rated breakdown voltage. For Schottky diodes, this leakage current is generally higher than other power devices. The main reasons for this are the thermionic emission transport mechanism and space charge carrier generation, both decrease rapidly at low operating temperatures. This can be seen from the reverse leakage current density ( $J_R$ ) equation, which can be expressed as a function of the reverse



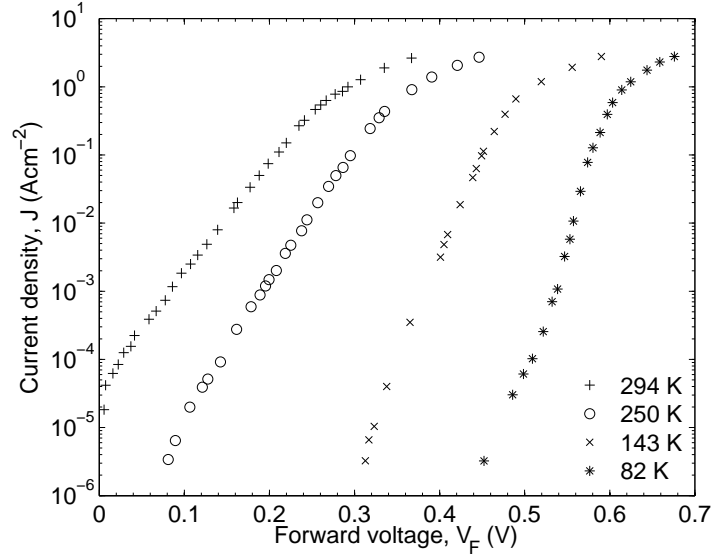


Figure 2.3: Previously measured forward current density against forward voltage of the Schottky diode BYS 26-45 (Seimens) by Simeonov and Kafedjiiska at different temperatures [12].

bias voltage ( $V_R$ ) [15]:

$$J_R = A^* T^2 \exp\left(-\frac{q\phi_{bn}}{kT}\right) \left[ \exp\left(-\frac{qV_R}{kT} - 1\right) \right]. \quad (2.4)$$

From the above equation,  $J_R$  is very sensitive to temperature due to their exponential relationship. The reverse characteristics of the power Schottky diode were studied by Singh and Baliga [16]. Fig. 2.4 presents their measured data of the reverse leakage current density of a Schottky diode rated at 500 V. The figure shows that even at high voltage, the reverse leakage current density is at least two orders of magnitude smaller at 77 K compared with 300 K.

### 2.1.1.2 PiN Diodes

PiN diodes were the first power devices developed, hence they have a long development history. They can be found in a huge range of applications with voltage ratings up to several kV and rated currents up to several kA that are commercially available. It is difficult to find any other type of diodes that operate at such a high voltage range. Fig. 2.5 presents a

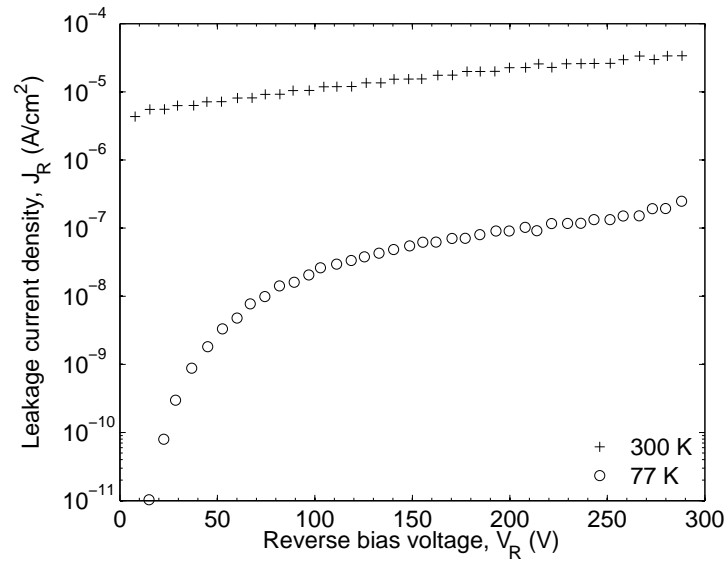


Figure 2.4: Previously measured reverse leakage current density of a power Schottky diode with reverse bias voltage at 300 K and 77 K, measured by Singh and Baliga [16].

typical PiN diode structure.

The name PiN describes the basic structure of the diode. Unlike a normal PN junction diode, there is a drift region (i-layer) in between the P and N regions. The drift region is an almost intrinsic, lightly doped Si layer, hence the name. It is this extra layer that gives the PiN diode its high voltage blocking capability. Generally speaking, the thicker or lower doped this layer is, the higher the blocking voltage. However, intrinsic Si has a high resistivity which leads to high conduction losses. The PiN diode is able to compensate for this by injecting a high level of minority carriers conductivity modulating the drift region. Therefore it is a bipolar device. The increase in charge carriers in the drift region dramatically reduces the resistivity of the device. One of the main disadvantages of the PiN diode is the relatively slow turn off time. This is due to the time required to remove all the excess charge carriers from inside the drift region which are present as a result of the conductivity modulation.

The conductivity modulation mechanism found in the PiN diode is a very complex process and the detailed mechanism is beyond the scope of this introduction, however it can be

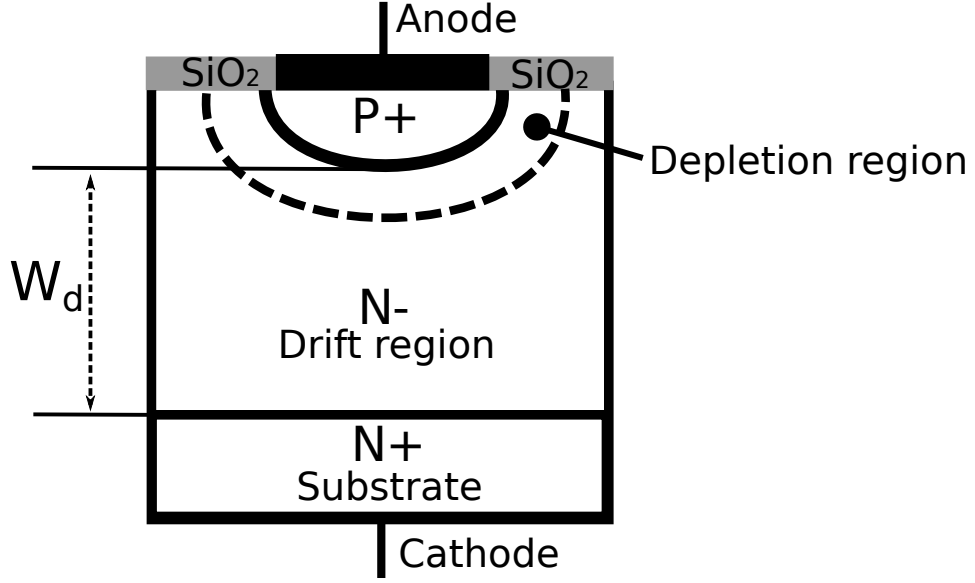


Figure 2.5: A typical PiN diode structure showing the P+N-(i)N+ structure and  $W_d$  as the drift region thickness.

approximated by several simple equations. The forward voltage,  $V_F$  can be expressed as:

$$V_F = V_J + V_d + I_F R_s, \quad (2.5)$$

where  $V_J$  is the voltage across the P+N- junction and can be approximated as [17]:

$$V_J \approx \frac{kT}{q} \ln \left( \frac{J_F}{J_S} \right), \quad (2.6)$$

$J_S$  is the saturation current, which is dependent on the intrinsic carrier concentration ( $n_i$ , see Chapter 3.1).  $V_d$  is the voltage across the drift region and can be approximated as [17]:

$$V_d \approx \frac{W_d^2}{(\mu_n + \mu_p)\tau}, \quad (2.7)$$

$R_s$  is the series resistance,  $W_d$  is the thickness of the drift region (see Fig. 2.5),  $\mu_n$  and  $\mu_p$  are the electron and hole mobilities (see Chapter 3.2) and  $\tau$  is the excess carrier lifetime. Variables such as the intrinsic carrier concentration and carrier mobilities are dependent on both temperature and dopant concentration.

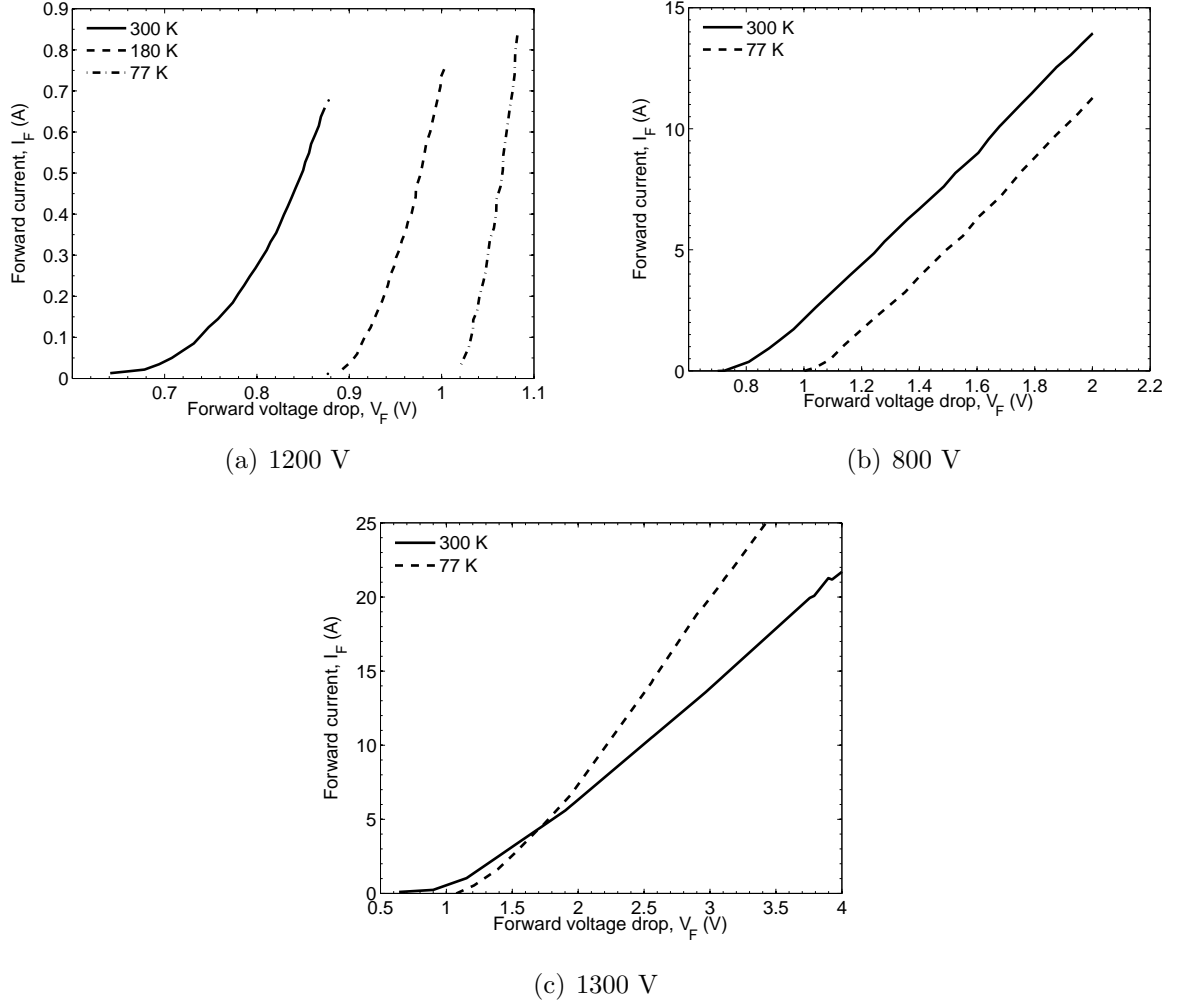


Figure 2.6: Forward voltages of three different PiN diodes: (a) 1200 V PiN diode, measured by Singh and Baliga [18]. (b) 800 V, 20 A PiN diode (20ETS08) [19] and (c) 1300 V, 5 A PiN diode (BYT106-1300) measured by Taylor et al. [19]

The temperature dependence of  $V_F$  has been investigated in a number of studies. Fig. 2.6 presents a selection of measured  $V_F$  for three different PiN diodes at temperatures down to 77 K. For all three PiN diodes, the PN junction voltage ( $V_J$  or forward knee voltage, see Fig. 2.1.) increased with decreasing temperature to over 1 V at 77 K. The increase in  $V_J$  is predicted by Eqn. 2.5 and 2.6, since  $J_S$  would decrease dramatically due to  $n_i$  which is a temperature sensitive parameter (see Chapter 3.1). Fig. 2.6(a) and 2.6(c) exhibited major improvements in the forward voltage drop at high current levels resulting from the increased slope of the IV curve. Interestingly, this behaviour was not exhibited in Fig.

2.6(b). The slope remained similar at the two temperature measurements with no indication of any improvements in the forward voltage at lower temperatures. This suggests that improvements in forward behaviour may not be universal across all PiN diodes.

The cryogenic reverse recovery of PiN diodes has also been extensively investigated. Fig. 2.7 presents two samples of previously measured data. Both PiN diodes exhibited considerable improvements in the turn-off time and reverse peak currents. This is due to reduced stored charged in the drift region at lower temperatures. The improvements in the reverse recovery characteristics allow higher switching frequencies, as well as much lower switching losses.

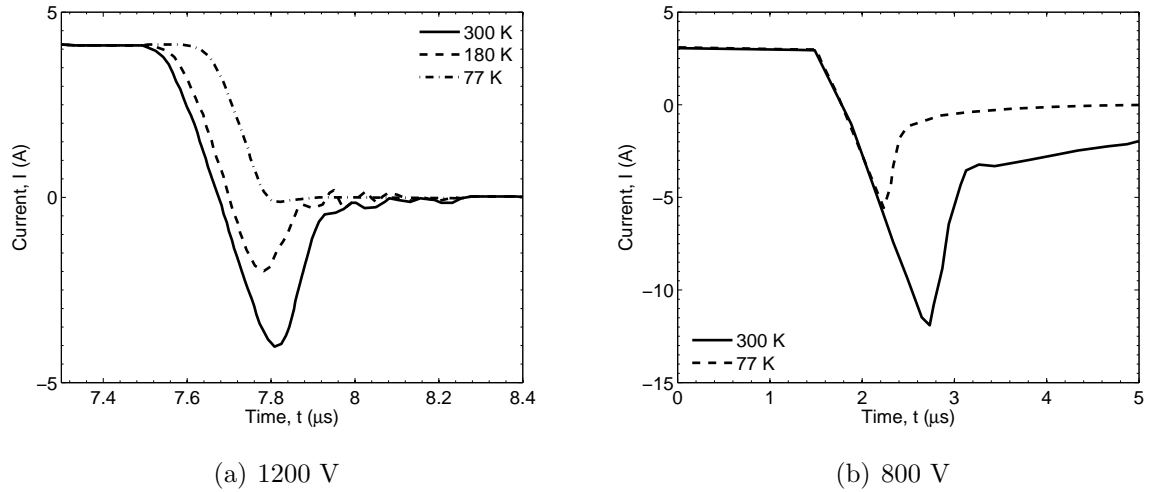


Figure 2.7: Previously measured turn-off characteristics of two different PiN diodes down to 77 K: (a) 1200 V PiN diode by Singh and Baliga [18] and (b) 800 V PiN diode by Taylor et al. [19]

The breakdown process of the PiN diode occurs at the PN junction and the breakdown voltage is dependent on the device structure and dopant concentration of the drift region (see Chapter 3.3). The cryogenic breakdown behaviour of a PiN diode is shown in Fig. 2.8 [19], the breakdown voltage was found to decrease at lower temperatures. At 77 K, the breakdown voltage reduces to approximately 60 % of the breakdown voltage at 300 K.

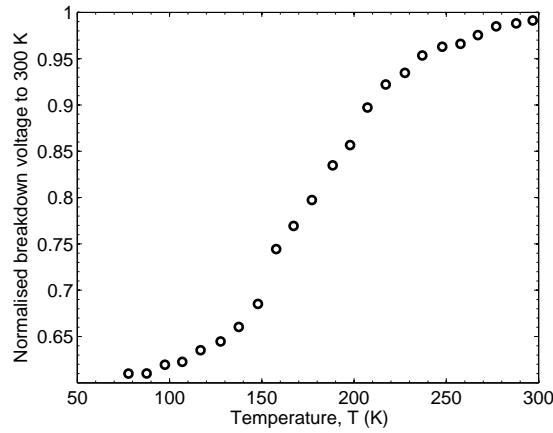


Figure 2.8: Previously Measured reverse breakdown voltage of a PiN diode (BY229-800A) normalised to 300 K by Taylor et al. [19]

### 2.1.1.3 Hybrid Power Diodes

Hybrid power diodes such as trench MOS barrier Schottky (TMBS) and merged PiN Schottky (MPS) diodes combine different technologies together in order to improve on the conventional power Schottky and PiN diode designs. These devices allow new trade-offs to be examined in terms of reverse leakage, switching speed and forward voltage drop. Fig. 2.9 presents the typical device structures of (a) TMBS diode and (b) MPS diode.

The TMBS diode can be described as a Schottky diode with MOS trench structures, during reverse blocking the trenches help grow the depletion region to shield the Schottky junction. This increases the breakdown voltage and reduces the reverse leakage current. Since the structure is capable of higher blocking voltages, the drift region dopant concentration can also be slightly increased and thereby reducing the drift region resistance [20]. However, by adding the MOS trench structures, the size of the active area is reduced.

As the name suggests, the Merged PiN Schottky (MPS) diode is a PiN diode and a Schottky diode merged together [21]. The structure is very similar to a normal power Schottky diode. However, in the MPS the P+ guards rings are no longer left floating but become part of the conduction path. The MPS incorporates the main advantages from the PiN structures and from the Schottky junctions. The resulting device has a lower breakdown voltage and a higher on-state resistance than a PiN diode but has a lower threshold voltage

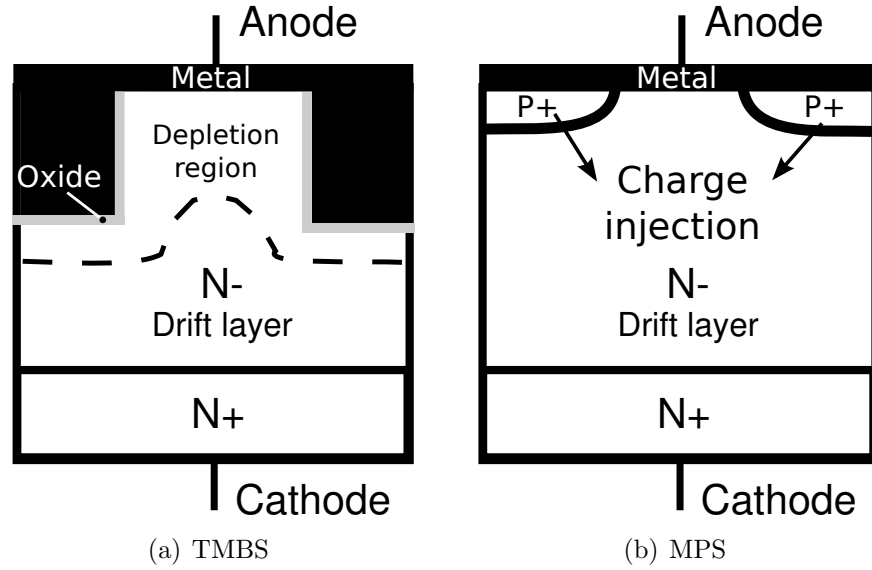


Figure 2.9: Illustrations of the typical structures of (a) the TMBS diode (b) the MPS diode.

and much faster switching capability. The exact behaviour of the device depends on the exact ratio of the PiN and Schottky regions across the active area, higher breakdown voltage can be achieved with higher ratio of PiN regions and faster switching can be achieved with higher ratio of Schottky regions.

The cryogenic behaviour of TMBS and MPS diodes have not been found in any available literature.

### 2.1.2 Unipolar Transistors

For Si devices, unipolar transistors are mainly field effect transistors (FETs) that conduct via one type of charge carrier. In Si, they are largely divided into two families. The first are the insulated gate FETs and, the more common, the metal-oxide-semiconductor FETs (MOSFETs), which dominate the low/medium voltage application sector due to their ease of gate control and circuit integration. The second are the junction FETs (JFETs), they are less common and are generally used in niche applications.

The general IV characteristics of an n-type power MOSFET are presented in Fig. 2.10. For p-type, the IV characteristics are inversely mirrored where the forward characteristic is in third quadrant and the reverse characteristic is in the first quadrant. The forward IV can

be split into two distinct regions: The linear region and the saturation region. The linear region follows ohms law until the voltage/current reach the saturation region and the current becomes constant with increase applied voltage. In reality, there is a limit to the maximum applied forward voltage in the saturation region before the device becomes over-stressed. For MOSFET,  $V_{G1} > V_{G2} > V_{G3} > V_{G4}$ . For normally-on JFETs,  $V_{G4} > V_{G3} > V_{G2} > V_{G1}$ . However, unlike the power MOSFET, a JFET does not have a reverse body diode. The third quadrant of a JFET IV characteristics is an inverse mirror of the first quadrant behaviour.

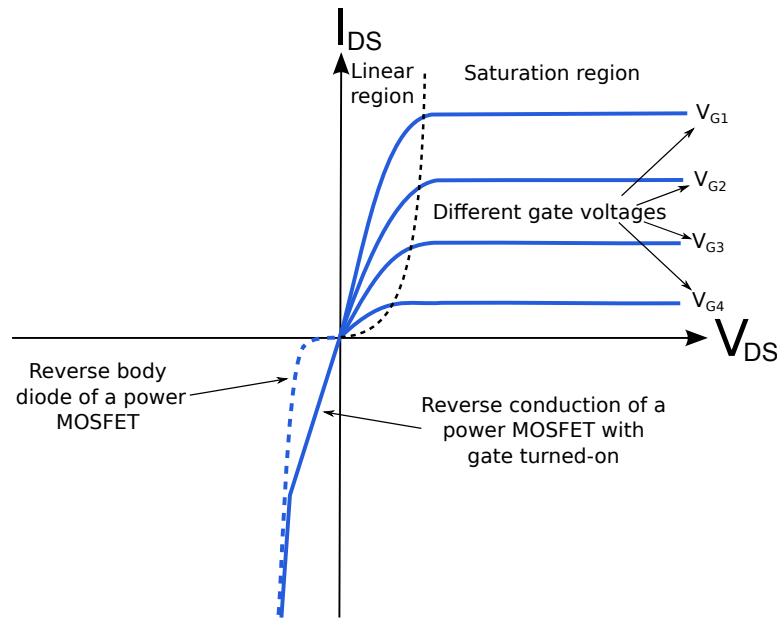


Figure 2.10: The generic IV characteristic of a power MOSFET.

### 2.1.2.1 Power Junction Field Effect Transistors

Power JFETs are commonly normally-on devices, which means current conducts through the device when there is no bias at the gate terminals. They can be made into normally-off devices but their performance is relatively poor compared to other types of transistors. The name junction FET comes from the PN junction used to deplete the channel region in order to turn off the device, hence it is a depletion mode device. A typical power JFET structure is shown in Fig. 2.11. The power JFET has no forward threshold voltage, this is due to the absence of a PN junction in the current conduction path. The current flows through the



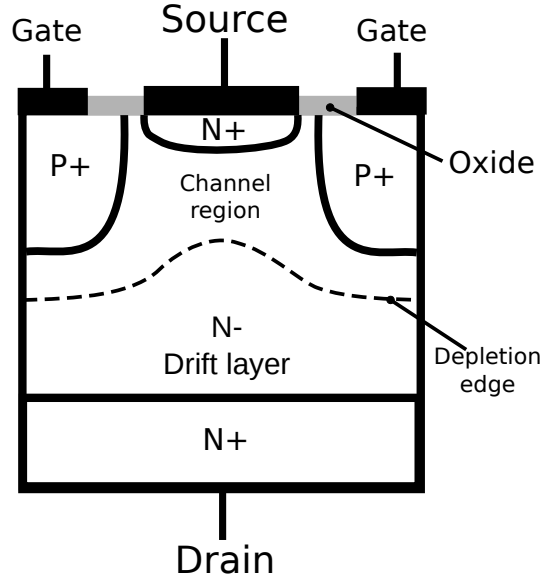


Figure 2.11: The typical structure of a power JFET, showing pinch-off of the channel region and the formation of the depletion edge into the drift region during turn-off.

N+N-N+ structure, with the forward voltage dropping mainly across the drift and channel region, hence  $V_F$  for power JFET can be expressed as:

$$V_F = I_F R_{drift} + I_F R_{chan} + I_F R_s. \quad (2.8)$$

$R_{chan}$  is the channel resistance which is dependent on the gate voltage and  $R_s$  is the series resistance. The device is turned off by applying a negative bias on the gate which depletes the channel region until the depletion regions merge together and pinch off occurs, blocking any further conduction. The power JFET is capable of bipolar conduction since forward biasing the gate beyond the threshold voltage of the PN junction would enable conductivity modulation, this characteristic is unwanted in most applications and the gate voltage is generally kept below 0.7 V.

The cryogenic behaviour of a 200 V power JFET was measured by Singh and Baliga down to 77 K [22]. The on-state resistance and forward blocking voltage are shown in Fig. 2.12. At 77 K, the on-state resistance at the linear region of the IV curve was shown to be approximately 12 % of the room temperature value and the forward blocking voltage was shown to decrease to approximately 85 % of the room temperature value.

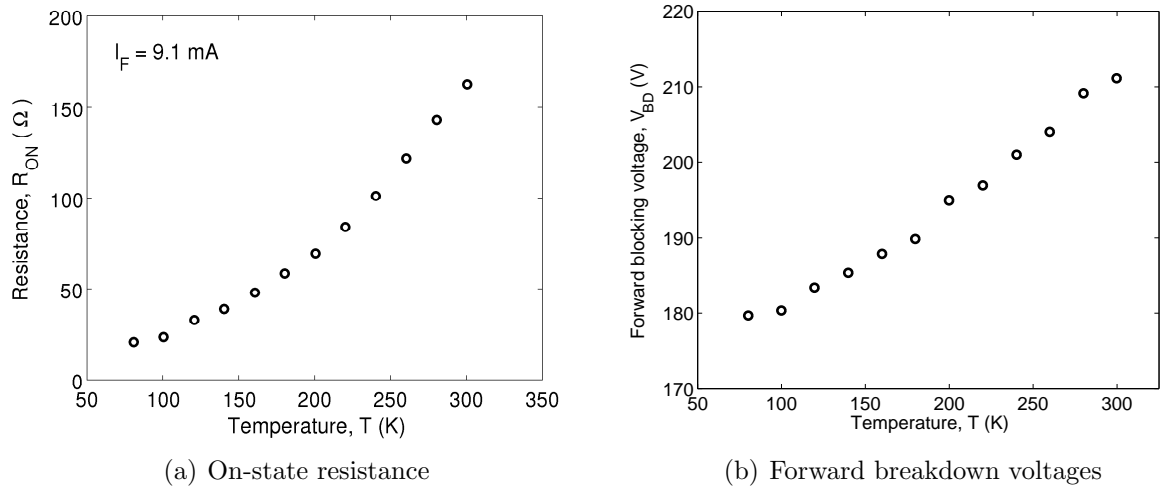


Figure 2.12: Previously measured (a) on-state resistance and (b) forward breakdown voltages of a 200 V power JFET at cryogenic temperatures by Singh and Baliga [22].

### 2.1.2.2 Power Metal Oxide Semiconductor Field Effect Transistors

Power MOSFETs were developed in order to take advantage of the high speed switching MOSFET structure used in integrated circuits. The MOSFET structure was redesigned to handle much higher voltages by adding a drift region similar to that seen in Schottky and PiN diodes. Power MOSFETs can be fabricated laterally or vertically. However, it is easier to conduct higher current with vertical device. Therefore, lateral power MOSFETs are generally designed for lower power applications only. They are normally off devices and are voltage controlled. The applied gate bias needs to be above the gate threshold voltage in order to turn on the device. The forward I-V characteristics are similar to the power JFET, the device can be operated in the linear (ohmic) region or the saturated (variable voltage/constant current) region. Fig. 2.13 illustrates the typical structure of a vertical power MOSFET. There are also more advanced structures such as: U-MOSFETs (Trench), cell optimised structures like HEXFETs® [23] and super-junctions (SJ) MOSFETs.

When the voltage applied to the gate exceeds the gate threshold voltage, an inversion layer (channel) is created in the P-well underneath the gate oxide. This is due to the field effect of the MOS structure, operating in a similar manner as a capacitor. The field is such that electrons are attracted to the surface. These are supplied from the n-type source/drain

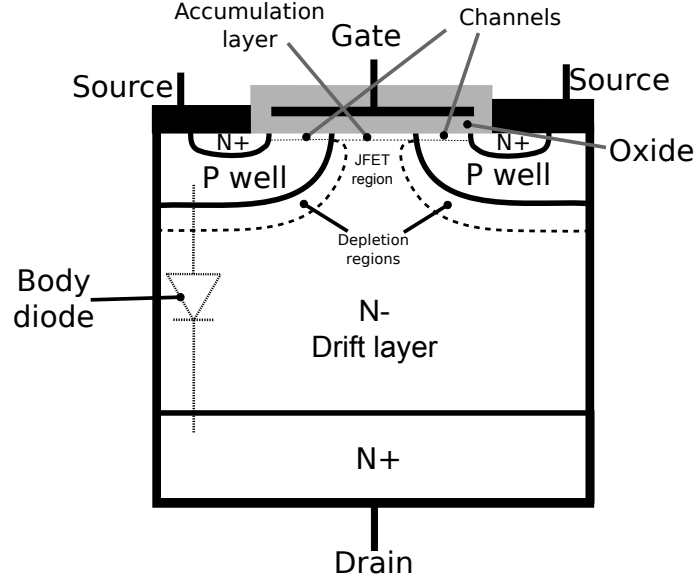


Figure 2.13: The typical structure of a vertical power MOSFET.

to form the thin but highly conductive inversion (channel) layer. At the same time, the gate bias will also cause an accumulation layer of electrons to form under the gate at the top of the JFET region. When there is a potential difference between the drain and the source, electrons will flow through the device. However, since there is a reverse biased PN junction at the JFET region, the depletion layer will restrict the current flow. The forward voltage ( $V_F$ ) consists of:

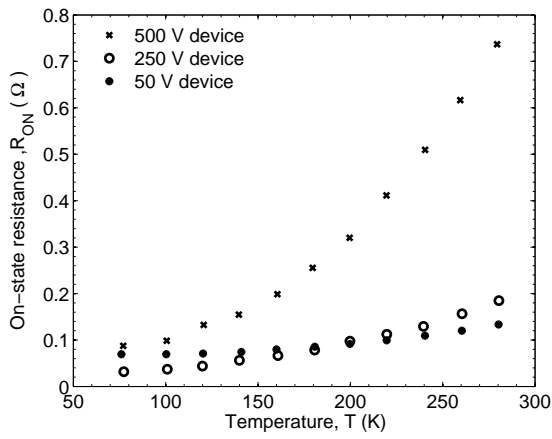
$$V_F = I_F R_s + I_F R_{chan} + I_F R_{accum} + I_F R_{JFET} + I_F R_{drift}. \quad (2.9)$$

$R_{accum}$  is the resistance of the accumulation layer and  $R_{JFET}$  is the resistance of the JFET region. All other parameters have been previously defined. The device can be switched off by removing the gate bias, when that happens, the channel can no longer be sustained. The electrons flow out of the P-well and the conduction path is removed, the reverse bias on the PN junction will expand the depletion regions until they merge and grow into the drift region.

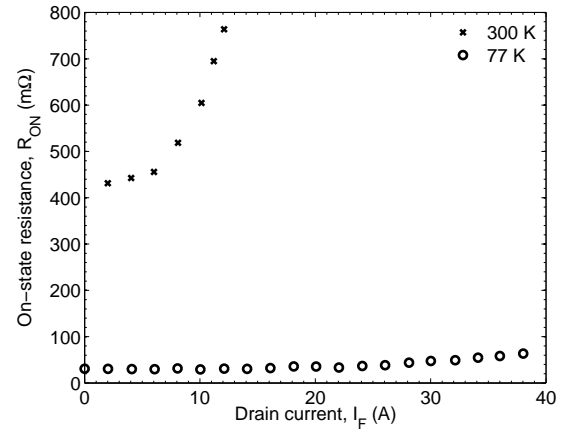
As shown in Fig. 2.13 and Fig. 2.10, the power MOSFET has an inherent body diode. Therefore, a power MOSFET can only block forward voltages, any reverse voltage above

## 2.1 Introduction to Silicon Power Devices and Cryogenic Behaviour

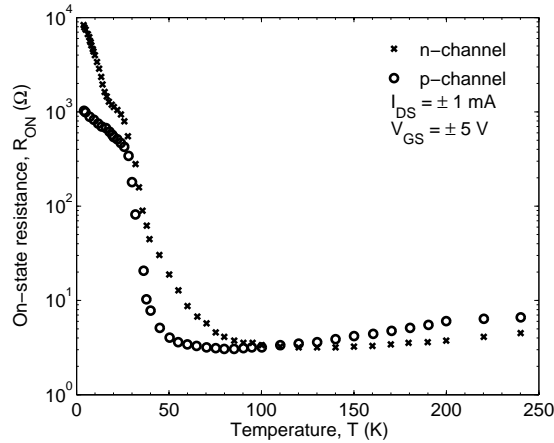
the threshold voltage of the body diode would lead to current being conducted in the reverse direction. The body diode structure is akin to the PiN diode structure as discussed in the previous sub-section. Therefore it operates under bipolar conduction and will differ in switching speed compared to the power MOSFET. The current rating of the power MOSFETs can be increased by connecting similar devices in parallel, they are particularly suited to this as their on-state resistance has a positive temperature coefficient which would prevent any one device from conducting too much of current.



(a) DMOSFETs [24]



(b) APT 10053LNR 1000 V, 20 A [25]



(c) SIPMOS 200 V, 1.4 A [26]

Figure 2.14: Previously measured on-state resistance of (a) DMOSFETs at different rated voltages by Singh and Baliga [24], (b) APT 10053LNR, rated at 1000 V, 20 A with  $R_{ON} = 0.53 \Omega$ , measured by Mueller [25] and (c) p and n channel SIPMOS (Siemens), rated at 200 V, 1.4 A measured by Karunanithi et al. [26].

There have been numerous studies into the cryogenic behaviour of MOSFETs for CMOS applications [27] [28] [29], as well as strained Si MOSFETs [30]. In comparison, there have been relatively few studies into the cryogenic behaviour of power MOSFETs. The measured on-state resistances of power MOSFETs from two different studies are presented in Fig. 2.14(a) and 2.14(b). All the power MOSFETs in the study were measured at temperatures down to 77 K, with exception of the work by Karunanithi et al. who measured to 4 K shown in Fig. 2.14(c) [26].

Fig. 2.14(a) shows the measured on-state resistance of the three DMOSFETs at different rated voltages, all three power MOSFETs exhibited decreased on-state resistances as temperature was reduced from 300 K to 77 K. The temperature dependence appears to be linear between room temperature and 200 K but saturates at temperatures below 100 K. Fig. 2.14(b) shows the improved current handling capability of a 1000 V rated power MOSFET. For a drain current of 2 A, the on-state resistance appears to decrease by a factor of 14 between room temperature and 77 K. The device also appears to be able to handle at least twice the rated drain current at 77 K without serious degradation on the on-state resistance. Fig. 2.14(c) shows the on-state resistance of a 200 V n-channel and p-channel SIPMOS (Siemens Power MOS) measured at temperatures from 240 K down to 4 K. Both devices exhibited a similar decrease in on-state resistance compared to the previously discussed power MOSFETs. However, the on-state resistance increased by several orders of magnitude as the temperature was reduced past  $\sim 90$  K for the n-channel and  $\sim 70$  K for the p-channel MOSFET. This is most likely due to carrier freeze-out effects. However, no other measurements have shown degradation occurring at temperatures as high as 90 K for the n-channel power MOSFETs.

The gate threshold voltages and breakdown voltages of three DMOSFETs with different voltage ratings are presented in Fig. 2.15. The gate threshold voltages are dependent on the gate oxide thickness and dopant concentration of the P-well. The gate threshold voltages for all three MOSFETs were found to increase with decreasing temperature. They each exhibited a  $\sim 0.7$  V higher threshold voltage at 77 K than at 300 K. The breakdown voltages of all three power MOSFETs are shown to reduce with decreasing temperature. They each

exhibited a  $\sim 20\%$  lower breakdown voltage at 77 K than at 300 K.

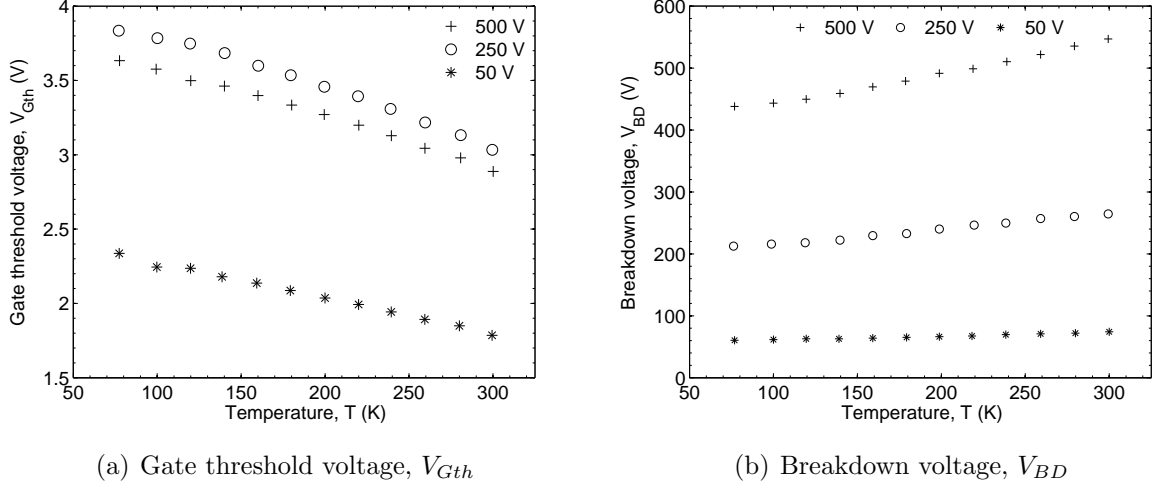


Figure 2.15: (a) Gate threshold voltages and (b) breakdown voltages of three different voltage rated DMOSFETs from room temperature down to 77 K, measured by Singh and Baliga [24].

### 2.1.2.3 Super-junction Power Metal Oxide Semiconductor Field Effect Transistors

The Super-junction is a relatively new concept which employs the charge-compensation principle to reduce the resistance of the drift region of a power MOSFET while maintaining the same breakdown voltage [31]. The Super-junction can reduce the on-state resistance below the ideal specific on-state resistance for Si, which was previously thought to be impossible. The Infineon CoolMOS<sup>TM</sup> was the first commercially available SJ power MOSFET [32]. Other SJ based structures have also been realised, such as STMicroelectronics's MDmesh<sup>TM</sup> [33].

Fig. 2.16 presents the basic structure of the SJ MOSFET. The main difference between SJ MOSFETs and conventional power MOSFETs are the alternatively stacked P and N pillars across the drift region. Assuming the pillar widths are relatively small, the two pillars compensate each other and the resulting reverse biased electric-field profile can sustain a much higher voltage by the formation of two dimensional depletion regions [34]. Therefore, the breakdown voltage is mainly dependent on the thickness of the drift region and less

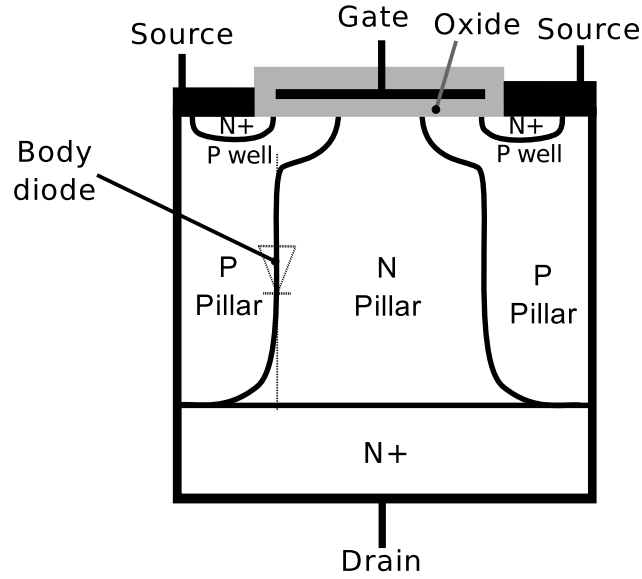


Figure 2.16: The typical structure of a SJ MOSFET.

dependent on the dopant concentration. The result is a device that can sustain higher voltage while reducing the on-state resistance by having a thinner drift region with higher dopant concentration. As shown in Fig. 2.16, the SJ power MOSFET also retains the function of the reverse body diode. The reverse body diode of the CoolMOS was found to switch faster compared to the conventional body diode of power MOSFETs [35].

The cryogenic behaviour of the CoolMOS was measured by Schlögl et al. down to the temperature of 80 K [36]. Fig. 2.17 presents their measured I-V characteristics and breakdown voltages for a 600 V, 20 A rated CoolMOS. No carrier freeze-out was observed above 80 K and the breakdown voltage decreased by  $\sim 20\%$  from room temperature to 80 K.

### 2.1.3 Bipolar Transistors

In general, bipolar transistors are three-terminal power devices that can sustain very high voltages. In order to reduce the resistance of the drift region, they employ conductivity modulation which operates with both types of charge carriers: holes and electrons. The conduction process mainly involves the bi-directional diffusion from high carrier concentration regions to low carrier concentration regions. Therefore the temperature dependent carrier concentration value is very important for bipolar transistors. This section will introduce and

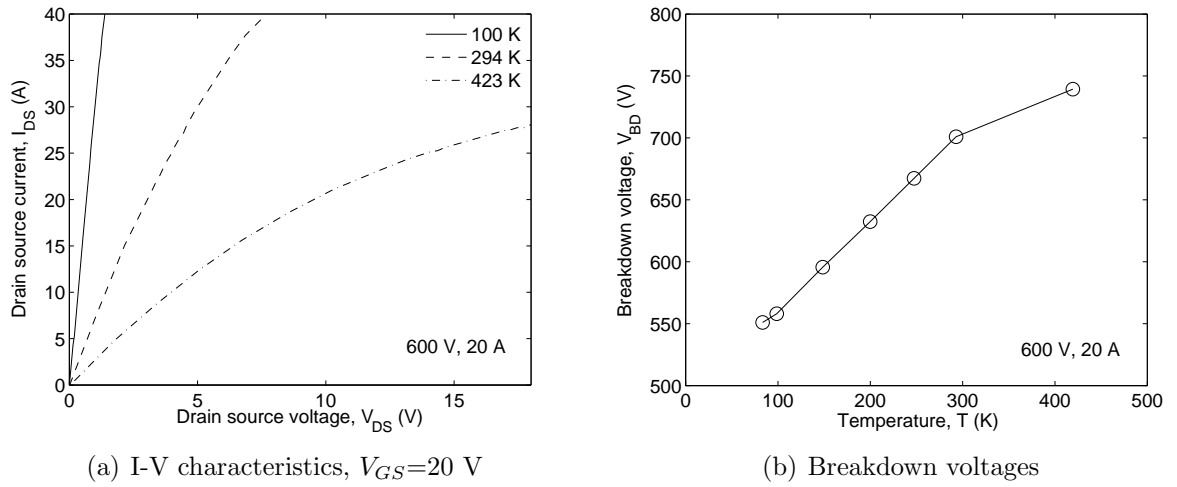


Figure 2.17: The (a) I-V characteristics and (b) breakdown voltages of a 600 V, 20 A rated CoolMOS™ from 423 K down to 80 K, measured by Schlögl et al [36].

present the known cryogenic behaviour of bipolar transistors such as: power bipolar junction transistors (BJTs), insulated gate bipolar transistors (IGBTs) and thyristors.

### 2.1.3.1 Power Bipolar Junction Transistors

Power BJTs are current controlled power devices, this means that sufficient current has to be injected into the base in order to turn on the device. The general IV characteristic of an NPN power BJT is presented in Fig. 2.18. The forward behaviour is quite similar to the unipolar transistor presented in Fig. 2.10, however the conduction mechanism is different and hence different names are assigned to the different regions. At low forward voltage, the device operates in the saturation region and at high forward voltage, it operates in the active region. There is an additional quasi-saturation region in the transition between saturation and active region. The current gain ( $\beta$ , the ratio between the input base current and the emitter current) of a power BJT is relatively low, therefore they are commonly arranged into a Darlington pair. This increases the current gain as well as reducing the drive current requirements. The power BJT is becoming less common as it has been superseded by other power devices such as power MOSFETs and IGBTs which are simpler to control. However, like the power JFET, they can still be found in a few applications and especially in research



of new semiconductor materials such as SiC.

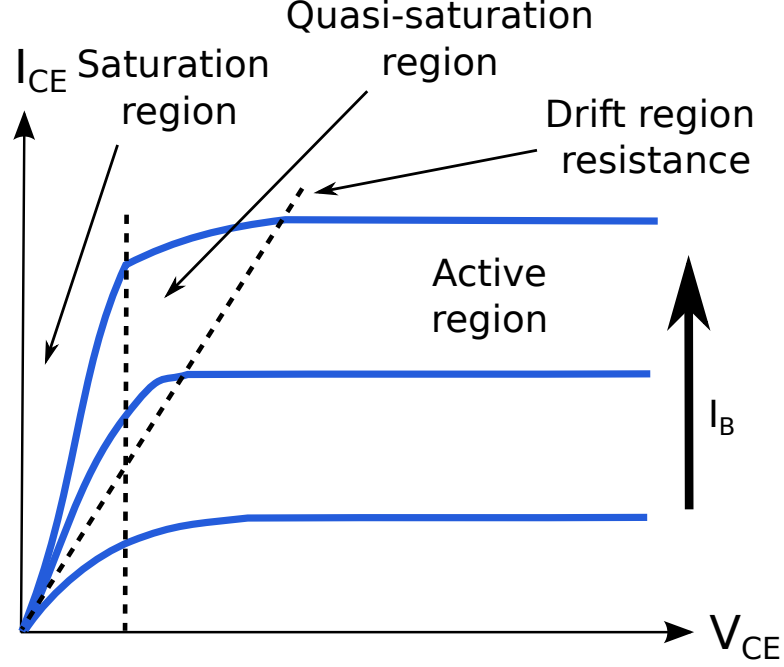


Figure 2.18: The generic forward IV characteristic of an NPN power BJT.

The typical structure of an NPN power BJT is presented in Fig. 2.19, the opposite PNP structure is also possible. When the collector-emitter is forward biased, depletion regions are formed on both sides of the PN- junction. Injection of the base current ( $I_B$ ) into the P region will diffuse into the depletion region and effectively neutralise it. Current can then flow through the device. The collector current ( $I_C$ ) can be expressed as [37]:

$$I_C = \beta I_B + I_{CEL} \quad (2.10)$$

$I_{CEL}$  is the leakage current when the collector junction is reverse biased.  $\beta$  is an important parameter since it determine the efficiency of the power BJT.

The cryogenic behaviour of a 500 V power BJT was measured by Singh and Baliga [38], their measured current gain for three different saturated current levels are shown in Fig. 2.20(a). All three current gains were shown to decrease, by an order of magnitude or more from 300 K to 77 K. The serious degradation in current gain for the power BJT at cryogenic

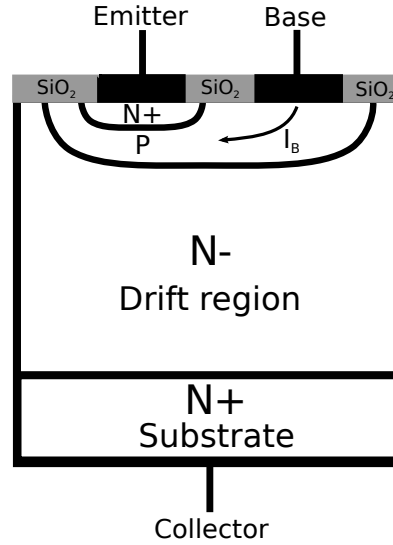


Figure 2.19: The typical structure of a power BJT.

temperatures will diminish the effectiveness of the device. The voltage drop across the base-emitter and collector-emitter at  $I_C = 1$  A is shown in Fig. 2.20(b). The base-emitter voltage increases from 0.9 V to 1.4 V while the collector-emitter voltage increases from 0.09 V to 0.2 V as the temperature was reduced from 300 K to 77 K. However, their work indicates that the switch-off time of the measured power BJT decreased at lower temperatures meaning the device can switch at higher frequencies.

### 2.1.3.2 Insulated Gate Bipolar Transistors

IGBTs are voltage controlled devices and they generally used in applications that require high voltage blocking capabilities. The advantages of having both simple gate drives requirements and relatively low on-state losses have made IGBTs very popular amongs high power applications. During high current conduction, the on-state forward voltage drop is lower compared to conventional power MOSFETs of the same voltage ratings and size. The general IV characteristic of an IGBT is presented in Fig. 2.21. The behaviour is similar to a power MOSFET with the exception of an additional forward junction voltage. The IGBT is also designed to block voltages in both the forward and reverse direction. The basic structure of the punch-through (PT) IGBT is shown in Fig. 2.22(a).

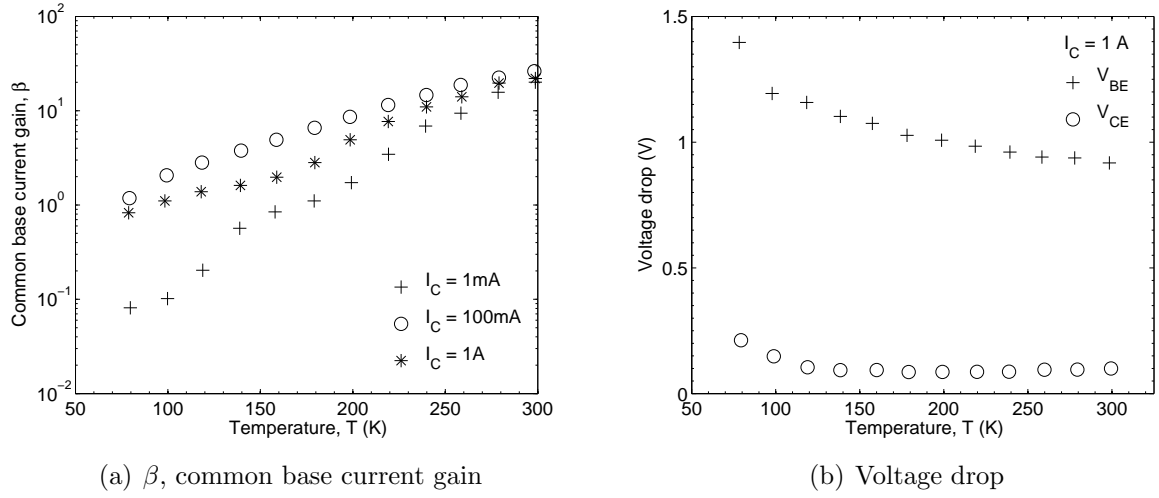


Figure 2.20: The (a) common base current gain at different saturation current levels and (b) the base-emitter and collector-emitter voltage drop at  $I_C = 1$  A, for a 500 V, 4 A rated power BJT from 300 K to 77 K, measured by Singh and Baliga [38].

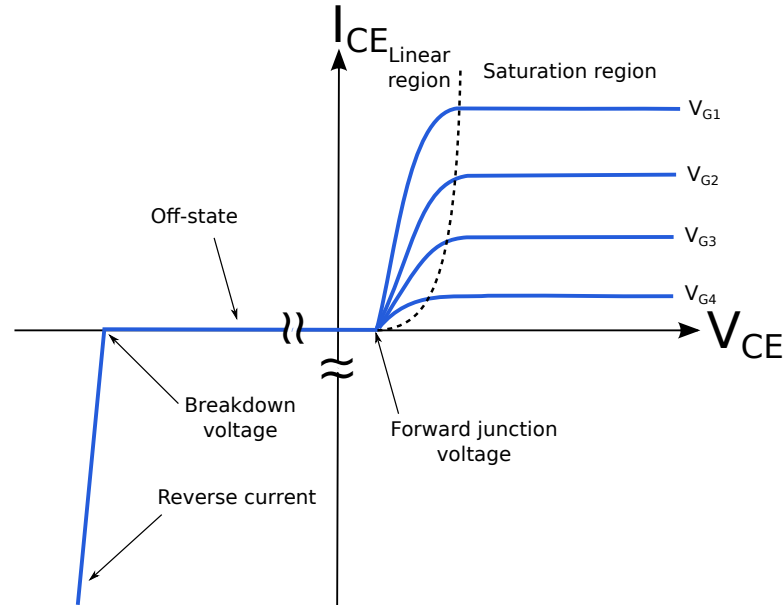


Figure 2.21: The general IV characteristic of an IGBT.

The structure of the IGBT is similar to a conventional power MOSFET, they both utilise the MOS structure for voltage control of the gate. The main difference is the use of an extra P+ layer that connects to the collector in the IGBT. The result is a device that operates in a very different manner. During on-state, electrons are injected into the drift region via

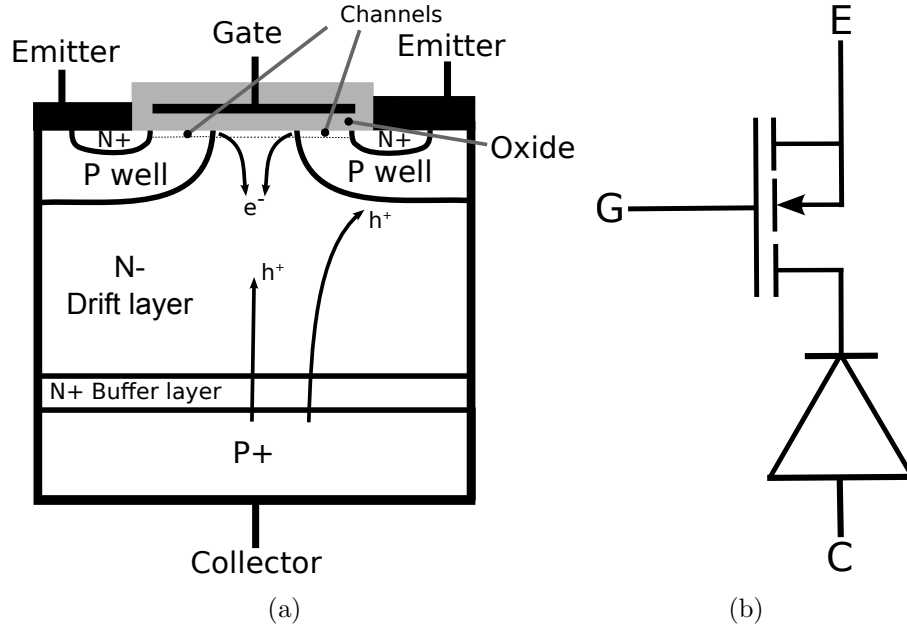


Figure 2.22: (a) The basic structure of an IGBT and (b) a simple equivalent circuit.

the channel; at the same time, the forward bias on the collector causes holes to be injected into the drift region. This enable conductivity modulation to take place and reduces the overall on-state resistance of the device. However, this also leads to longer turn-off times in comparison to the power MOSFETs. The slower turn-off is due to the need to remove the excess charge carriers from the drift region. This characteristic of the IGBT makes it less suitable for very high speed switching applications. The N+ buffer layer is used in a punch-through device, where the depletion region reaches the buffer layer during the blocking state. They are generally found in lower voltage IGBTs ( $<1200$  V), whereas IGBTs without the N+ buffer layer are known as non-punch through (NPT) and are found in higher voltage rating devices. As shown in Fig. 2.22(b), the IGBT can be viewed as a MOSFET in series with a PiN diode. The PiN diode is not obvious within the IGBT structure but when the inversion layer is created under the gate, the conduction path is effectively P+N-(N-channel)N+ (similar to the P+N-N+ structure of the PiN diode) [37]. More advanced IGBT structures include trench gate, injection enhanced modifications, selective lifetime controls and reverse conducting IGBTs.

The forward voltage ( $V_F$ ) of the IGBT is different compared to the power MOSFET.

Other than the voltage dropped across the drift region and channel, the IGBT has an additional PN junction threshold voltage ( $V_J$ ). The forward voltage has to be above this threshold voltage before the device can conduct (just like the threshold voltage of the PiN diode in Eqn. 2.6). This is the reason why at the same voltage rating, the forward voltage of the MOSFET is lower than the IGBT at low current levels.

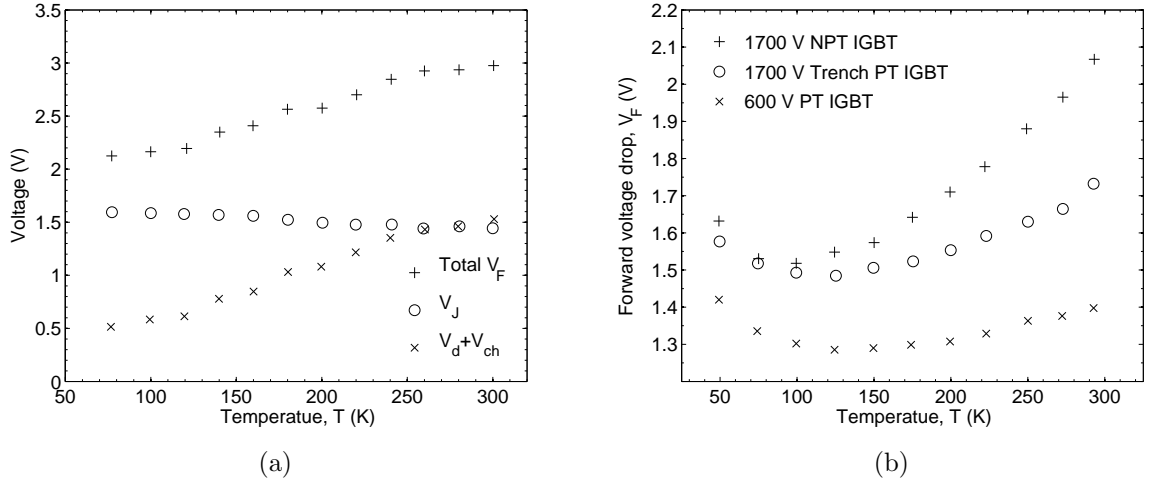


Figure 2.23: (a) Forward voltage of an asymmetric n-channel IGBT, showing the temperature dependence of the junction voltage ( $V_J$ ) and the voltage drop across the drift and channel region ( $V_d + V_{ch}$ ), measured by Singh and Baliga [39] and (b) the temperature dependent forward voltage of three different IGBTs, measured by Forsyth et al. [40].

The cryogenic behaviour of IGBTs have been measured in a number of studies [41] [39] down to 77 K. Further studies by Caiafa et al. [42] measured IGBTs down to 4 K and for more advanced IGBT structures, such as trench gate IGBTs down to 50 K [40]. The temperature dependence of the forward voltage of an n-channel IGBT is presented in Fig. 2.23(a) [39], the total forward voltage ( $V_F$ ) is shown to decrease at lower temperatures. However, The voltage drop across the PN junction ( $V_J$ ) was shown to increase at lower temperatures, limiting the reduction in the achievable forward voltage at cryogenic temperatures. The temperature dependent forward voltages of three different IGBTs are presented in Fig. 2.23(b) [40], these included punch-through (PT), non-punch-through (NPT) and trench devices. In this study, all three IGBTs have shown a reduction in the forward voltage, down to  $\sim 100$  K for the NPT IGBT,  $\sim 125$  K for PT IGBT and trench PT IGBTs. Below this temperature, the forward

voltage increases again.

The gate threshold voltage is mainly dependent on the gate oxide thickness and dopant concentration of the P-well. The temperature dependent gate threshold voltages of four different IGBTs are presented in Fig. 2.24(a), the gate voltages rise with decreasing temperatures. This is because the MOS structure of the IGBT is basically the same as the power MOSFET and similar behaviour has been shown in Fig. 2.15(a). The temperature dependent breakdown voltages of three different IGBTs were also measured by Forsyth et al. [40], the data are presented in Fig. 2.24(b). The temperature dependence of the NPT and PT IGBTs are similar to the power MOSFETs and reduce linearly by approximately 20-25 % from 300 K down to 77 K. However, for the trench PT IGBT, the breakdown voltage appears to drop by  $\sim 60$  % over the same temperature range in a non-linear fashion.

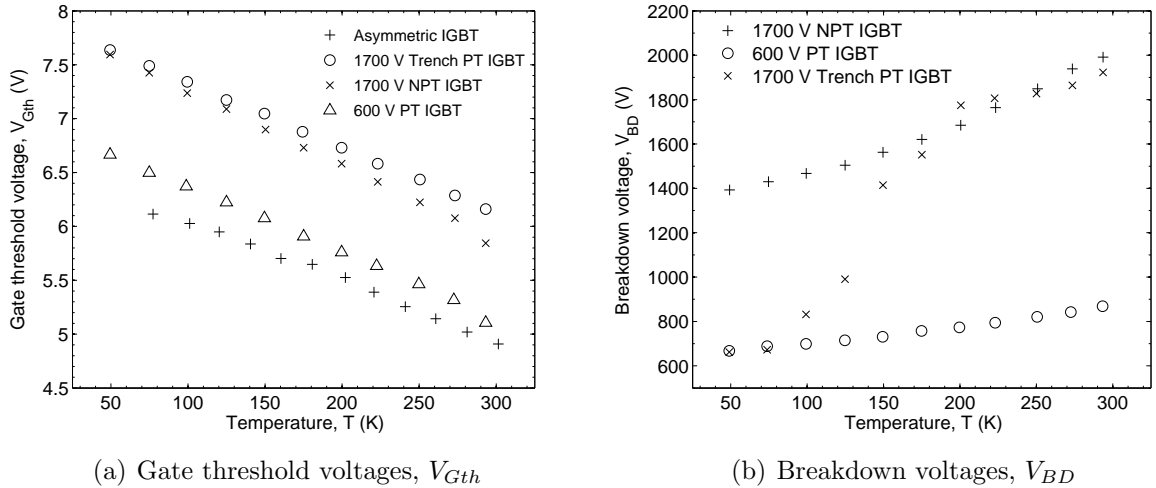


Figure 2.24: The temperature dependent (a) gate threshold voltages of four IGBTs (+ [39],  $\circ$ ,  $\times$ ,  $\triangle$  [40]) and (b) breakdown voltages of three IGBTs [40].

### 2.1.3.3 Thyristors

The thyristor, also known as silicon controlled rectifier (SCR), is a class of high power device that has the basic structure of four alternating P and N type Si layers, as presented in Fig. 2.25. It is a type of latching switch, which is turned on by an injection of current into the gate terminal. Once it is on, the gate loses control and the device stays on as long as the forward

current continues to flow. The device can be switched off either by reducing of the forward current below a threshold level commonly known as the *holding current* or applying a reverse bias across the device. The general IV characteristic of a thyristor is presented in Fig. 2.26. Similar to the IGBT, the thyristor has a forward junction voltage drop, which limits the minimum forward voltage. The figure also illustrates the forward blocking characteristics and the snap-back action when current is injected into the gate.

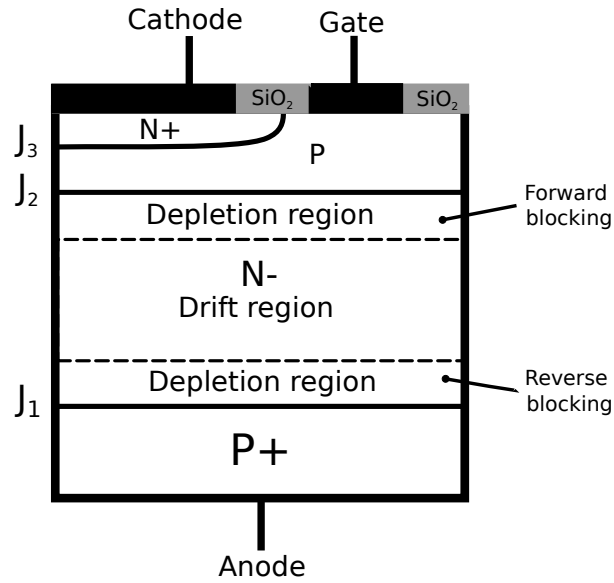


Figure 2.25: The basic structure of a thyristor.

There have been many advances in thyristor device structure design that have made the device more versatile and easier to control. The numerous classes of thyristor structure are quite extensive and can have very different characteristics compared to the original thyristor design. The main classes are gate turn off (GTO) thyristors, triode for alternating current (TRIAC), static induction thyristor (SITh), MOS controlled thyristor (MCT), emitter switched thyristor (EST), light triggered thyristors and reverse conducting thyristors to name but a few. During the off-state, a thyristor can block in both the forward and reverse direction with the two depletion layers shown in the figure. Technically, in the reverse blocking direction, the junction  $J_3$  is also reverse biased. However,  $J_3$  would breakdown much earlier than  $J_1$  due to the difference in the dopant concentration and thickness between the drift region and the N+ region.

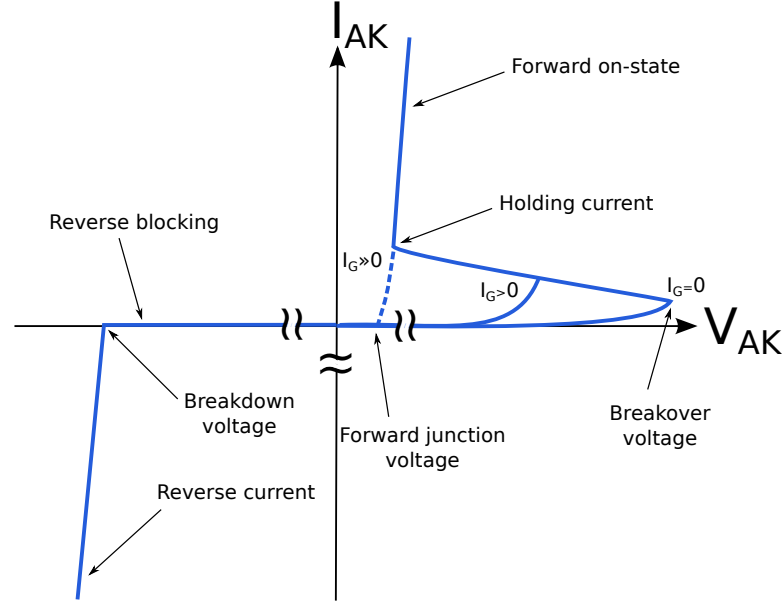


Figure 2.26: The general IV characteristic of a thyristor.

During on-state operation, conductivity modulation is used to reduce the resistivity of the N- drift region as well as the P region that is connected to the gate terminal. The forward voltage of the thyristor can be approximated as:

$$V_F = V_{J1} - V_{J2} + V_{J3} + V_d, \quad (2.11)$$

where the voltages across  $J_1$  and  $J_2$  effectively cancel each other out. The voltage drop is then across the  $J_3$  and the drift region, the voltage drop across the drift region should be relatively small due to the conductivity modulation process.

The cryogenic behaviour of thyristor was first measured by Menhart et al. from room temperature down to 93 K [43] [44]. The forward voltage drop of a 1200 V, 560 A thyristor at 125 A and 250 A are presented in Fig. 2.27(a). The temperature dependence of the forward voltage is not monotonic. From room temperature down to  $\sim 150$  K, it increased with decreasing temperature but reduced at temperatures below 150 K.

The gate threshold current,  $I_{Gth}$  is the minimum current required to turn on a thyristor. The  $I_{Gth}$  temperature dependence of a 1300 V, 420 A inverter thyristor is presented in Fig. 2.27(b), the gate threshold current also exhibited non-monotonic behaviour, it increases as



temperature is reduced from room temperature to  $\sim 170$  K and then decreases dramatically to 40 % of the value measured at room temperature as temperature is reduced further. Both the forward voltage drop and the gate threshold current were also measured by Singh and Baliga [16] for a 1300 V, 4 A thyristor (much lower rated current compared to Menhart's measurements). The temperature dependent forward voltage drop and gate threshold current were monotononic, both increased with decreasing temperature down to 77 K. This is in contrast to the data presented in Fig. 2.27(a) and 2.27(b). The temperature dependent breakdown voltages of the 1200 V inverter thyristor is also presented in Fig. 2.27(c), it shows an overall reduction with decreasing temperatures, down to 70 % of the breakdown voltage at 93 K compared to that measured at room temperature [43].

Static induction thyristors and emitter switched thyristors have also been measured at cryogenic temperatures. For the static induction thyristor, otherwise known as field controlled thyristor (FCT), the forward voltage drop of a 500 V device was found to have increased by 40 % from room temperature down to 77 K. The breakdown was found to decrease by 20 % over the same temperature range. Furthermore, the turn-off time reduced by ten times [45]. For the emitter switched thyristor, a reduction in the forward voltage drop was found in high current condition for a 1100 V device [46].

### 2.1.4 Discussion

From the known cryogenic behaviour of Si based power electronics, it is clear that they do operate at cryogenic temperatures. Most devices operate at temperatures far below their stated operating temperature range, and some even exhibited improvements at lower temperatures. However, degradations have also been observed. Furthermore, most of the studies only investigated device behaviour down to the liquid nitrogen temperature of 77 K. Behaviour below this temperature is unknown and is especially important as other effects such as carrier freeze-out will dominate. For the intended free-wheeling application, the operating temperature is 30 K. Therefore, it is imperative that the optimal device is chosen to achieve the lowest conduction loss and highest breakdown voltage. Comparison of the various devices will be discussed in the next section.

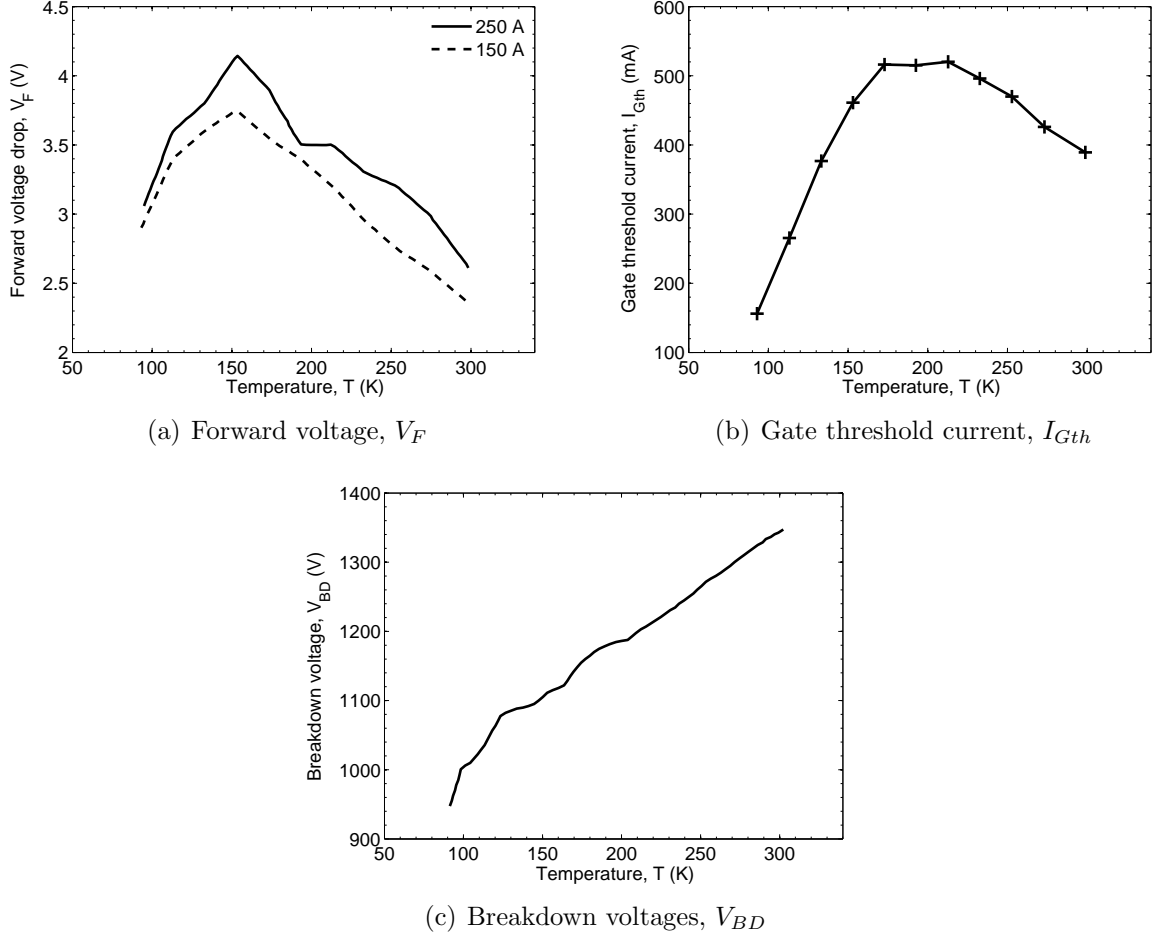


Figure 2.27: The temperature dependent (a) forward voltage at 125 and 250 A [43], (b) gate threshold current [44] (c) and breakdown voltages and of different thyristors [43]. All measured by Menhart et al.

### 2.1.4.1 Power diodes

As discussed in section 2.1.1, the two main classes of power diodes are power Schottky diodes and PiN diodes. The main difference between the two classes are their rectifying junction contacts. For the Schottky diodes, the threshold voltage is determined by the metal type. In all the measured cases, the threshold voltages of the Schottky device is lower than the PN junction. Therefore, at cryogenic temperatures the minimum voltage across the Schottky diode is always lower than the PiN diode leading to lower power loss capabilities. For this reason alone, Schottky diodes should be able to achieve higher efficiency compared to PiN

diodes. However, under high current conditions, the forward voltage of the Schottky diode ( $V_F$ ) could become higher than the PiN diode due to the increasing voltage drop across the drift region. Following this logic, the MPS hybrid diode should be superior to both device classes at cryogenic temperatures. The potential cryogenic behaviour of TMBS diode is uncertain and would require investigation.

### 2.1.4.2 Unipolar and Bipolar transistors

Bipolar devices discussed in section 2.1.3, which employ conductivity modulation are known to operate better at higher temperatures. This is because the conductivity of the drift region can be improved by raising the carrier concentration through rising temperature. The opposite occurs at low temperatures. Since carrier concentration reduces at lower temperatures, devices that rely on conductivity modulation becomes less effective. Unipolar devices, which operate with drift current only, show improvements in conductivity through increased carrier mobilities at lower temperatures. Furthermore, with the exception of the power BJT, all bipolar devices have a forward threshold voltage, this would limit the lowest forward voltage of the device. Even for the power BJT, the presented measurements have shown serious degradation in the common base current gain at lower temperatures, as well as degradation in the forward voltage of the device. For these reasons, bipolar devices are poorly optimised overall for cryogenic operations.

Within the unipolar transistor class, both power JFETs and power MOSFETs have shown significant improvements at cryogenic temperatures. However, power JFETs are harder to control, as they require active reverse blocking which would complicate the gate driver design. Also, since they are normally-on devices, they are unsuitable for the intended application of this work. Furthermore, it is difficult to find high power JFETs with breakdown voltages above 100 V. Power MOSFETs are therefore the most promising device for this study, the gate is easy to control, they are normally-off devices and both high voltage and high current devices are available. Power MOSFETs can also be connected in parallel to share current, which would reduce the forward voltage even further. Finally, more advanced power MOSFET structures like CoolMOS could be studied to investigate the potential benefits of

SJ technologies at temperatures below the liquid nitrogen temperature of 77 K.

## 2.2 Reliability Issues at Cryogenic Temperatures

The reliability of power device can be quantify using failure rates and the failure rate against time curve is commonly known as the bathtub curve (See Fig. 2.28). The curve describes the chance of a device failing through out the time it spent in operation. At the beginning of operation, the failure rate is high and this is known as infant mortality which is due to a number of reason such as undetected defects in devices. Once devices past this period, they enters a long period of useful life where a constant failure rate is found, mainly due to random failures. After this period, the device enters the wear out stage where the accumulated damage gained from the two previous periods increases the failure rate of the device.

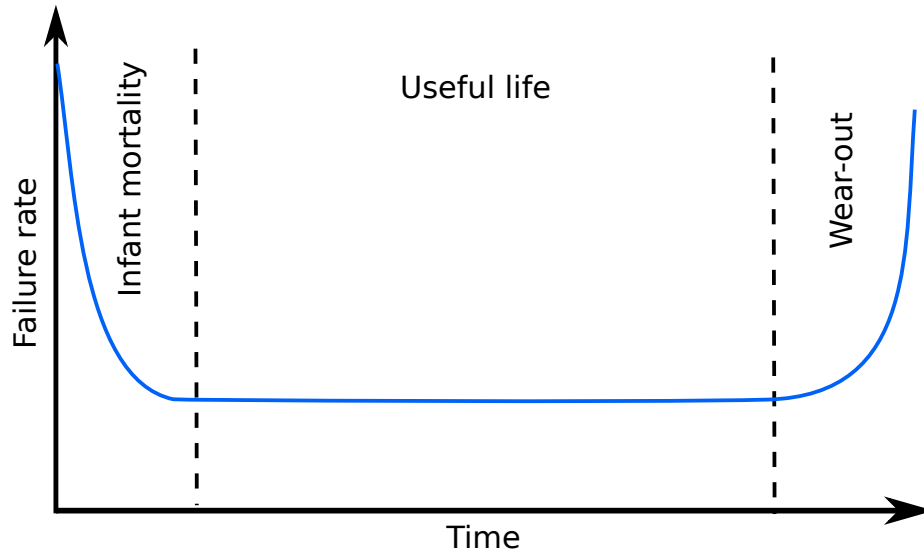


Figure 2.28: The reliability of electronic devices represented by the idealised graph commonly known as the bathtub curve [47].

Until now, the industrial requirement for cryogenic specified power electronic devices is minimal and no commercially available device was found to be qualitatively rated or tested for cryogenic operations. Therefore, failure rates of power devices at cryogenic temperatures are scarcely available for public use. Nevertheless, a brief introduction into the known or expected reliability issues of power devices will be presented in this section.

### 2.2.1 Thermal Expansion of Materials

One of the main concerns with operating power devices at cryogenic temperatures is the possible mismatch of coefficient of thermal expansion (CTE)  $\alpha$  within the device package, which could lead to thermal shock. Various materials that match well at room or higher temperatures could be severely mismatched at cryogenic temperatures. Even exposing the materials to cryogenic conditions for a short period of time could be enough to cause fractures or delamination. Furthermore, thermal cycling could also degrade attachments. Bond wire lift off, solder cracking and die delamination are some of the possible failure events for power devices.

Fig. 2.29 presents the measured CTE for pure copper [48] and intrinsic Si [49] down to  $\sim 20$  K. Although CTE becomes closer between the two materials at cryogenic temperatures, CTE actually becomes negative at temperatures below  $\sim 120$  K for Si. This means intrinsic Si actually contracts with increasing temperatures at this temperature range. Although the contraction is relatively small, it is unknown how this would affect the overall package of the device.

### 2.2.2 Silicone gel

In most common power modules, a soft silicone gel is commonly employed to encapsulate all the components within the casing. This is mainly used to protect against arcing, moisture and other contaminations. It has good thermal, electrical and mechanical properties at room and higher temperatures. However, it is known to degrade at lower temperatures and even solidify at temperatures as high as  $-60^{\circ}\text{C}$  [50], partial discharge and irreversible damage were also found to occur after long exposure to low temperatures.

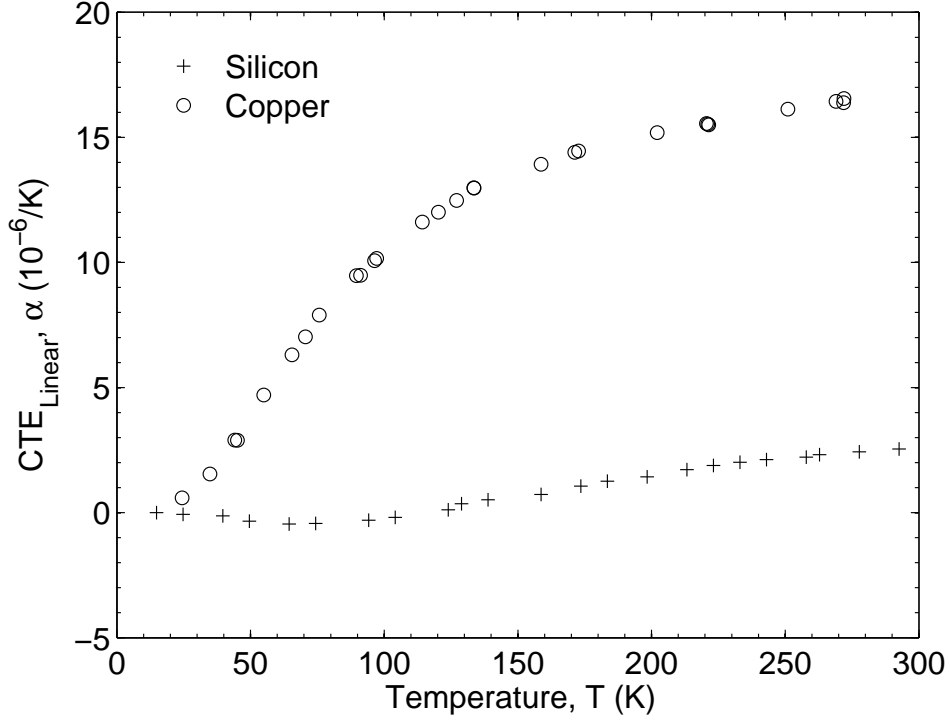


Figure 2.29: The temperature dependence of the coefficient of thermal expansion for pure copper [48] and intrinsic Si [49].

## 2.3 Introduction to Semiconductors Beyond Silicon

Although Si is still the dominant semiconductor in the power electronics industry, much of the current scientific, commercial and military research has been on other semiconductor materials that can operate beyond the limits of Si. This is because Si devices are not capable of operating at the extreme temperatures. At temperatures below 50 K, carrier freeze-out becomes a dominating effect in Si. At high temperatures, there is a practical upper operating limit between 150 and 200 °C when Si ceases to be a semiconductor due to the increase in intrinsic carrier concentration. Si also has a relatively low critical electric field when compared with some other semiconductor materials. This limits the achievable on-state resistance for Si devices. This section will discuss the possibility of using narrow band-gap (NBG) materials and wide band-gap (WBG) materials for cryogenic device operation.

### 2.3.1 Narrow Band-gap Materials

NBG materials can be defined as semiconductor materials that have a lower energy band-gap than silicon ( $<1.12$  eV). The main NBG materials are germanium (Ge) and its alloy with silicon known as silicon-germanium (SiGe). Ge is famously known as the material that gave birth to the first transistor. Although not commonly used for power devices, it is used in solar cell and light emitter diodes (LEDs). SiGe is a general term for an alloy ( $Si_{1-x}Ge_x$ ), which consists of both Si and Ge. Depending on the value of the mole fraction  $x$ , it can have behaviour anywhere between Ge and Si. Today it is used in hetero-junction transistors and strain induced complementary metal-oxide-semiconductor (CMOS) transistors.

The National Aeronautics and Space Administration (NASA) in collaboration with other commercial groups have been investigating the cryogenic behaviour of Ge and SiGe power devices for deep space missions, where satellites and other spacecraft are expected to experience temperatures as low as 20 K. For those applications, operating power circuits at cryogenic temperatures can avoid the need to warm up electronics which is normally implemented in Earth orbit satellites. Hence energy can be saved which would be crucial in the success of missions, as well as reducing overall cost. Ge and SiGe were chosen because of their lower carrier freeze-out temperatures compared to Si, as well as higher electron and hole mobilities.

SiGe devices including PiN diodes [51], BJTs, JFETs, IGBTs and metal-insulator-semiconductor-field-effect-transistors (MISFETs) have been developed by Ward et al. for space applications [52]. The same group has also characterised some commercially available Ge power diodes down to 4 K. The forward and breakdown voltages are presented in Fig. 2.30. The forward voltages at both 0.2 A and 4 A can be seen to increase with decreasing temperature. Interestingly the voltage difference between the two current points becomes closer temperature decreases. The breakdown voltages of the three Ge power diodes also exhibited an overall reduction with decreasing temperatures. SiGe power diode prototypes were also fabricated and measured down to 78 K, an example of the forward I-V characteristic are shown in Fig. 2.31(a). The diodes exhibited increased threshold voltages at lower temperatures but appear to saturate at temperatures below 173 K. Also, the on-state resistances appear

## 2.3 Introduction to Semiconductors Beyond Silicon

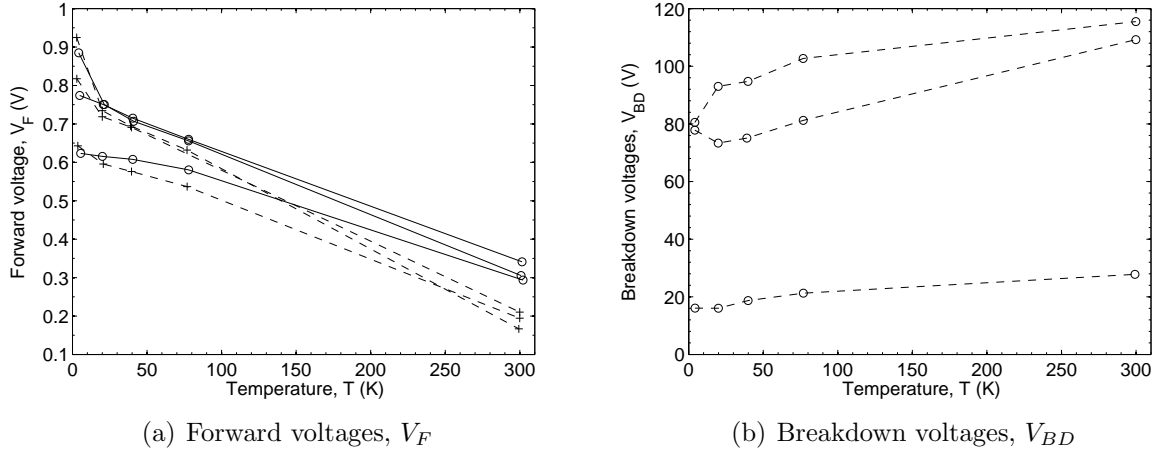


Figure 2.30: The previously measured temperature dependent (a) forward voltage at 0.2 A (+) and 4 A (O) and (b) breakdown voltages of three commercially available Ge power diodes, measured by Ward et al. [51].

to be fairly constant above 173 K but decrease at lower temperatures. SiGe hetero-junction bipolar transistors (HBT) were also fabricated and measured at cryogenic temperatures, Fig. 2.31(b) presents the IV characteristic from 358 K to 78 K. The HBT exhibited little improvement in operation at lower temperatures. The on-state resistance stays fairly constant but the saturation current decreases.

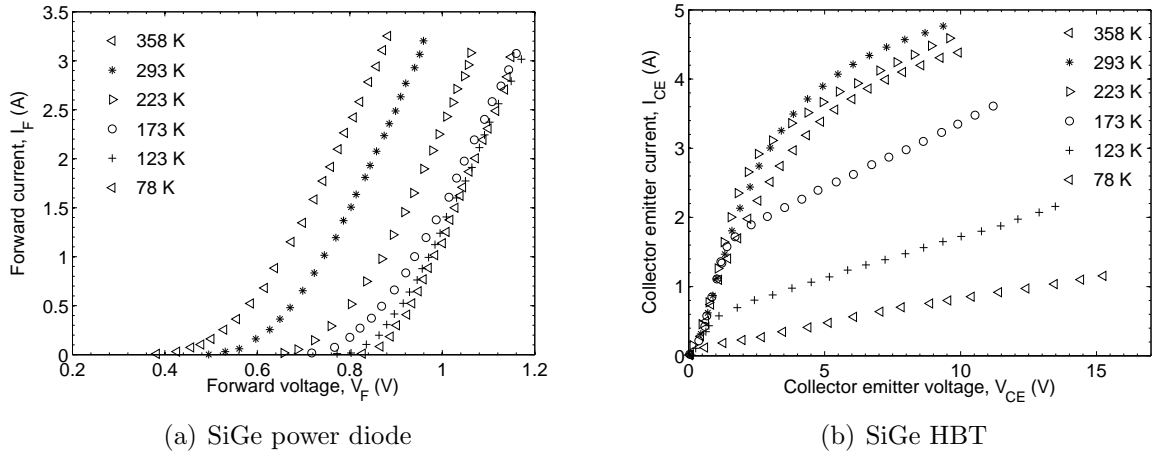


Figure 2.31: Temperature dependent I-V characteristics of (a) SiGe power diode and (b) SiGe HBT, measured by Elbuluk et al. [53].



### 2.3.2 Wide Band-gap Materials

WBG materials can be defined as semiconductor materials that have a higher energy band-gap than silicon ( $>1.12$  eV). The main WBG materials used in power devices are gallium arsenide (GaAs), silicon carbide (SiC) and gallium nitride (GaN).

GaAs is a III/V semiconductor with an energy band-gap (1.42 eV) which is slightly higher than Si. GaAs has a very high electron mobility which is why the use of GaAs has been well received in digital and microwave applications. Even though GaAs has a higher energy band-gap than Si, it is also known to operate well at liquid helium temperatures (4 K) [54]. One of the main reasons GaAs can operate at such low temperatures is because of its low dopant ionisation energy (see Chapter 3.2).

GaAs is superior to Si in many respects, however it has not been an emerging power electronic material due to a number of drawbacks. First, the thermal conductivity of GaAs is less than half of Si which means it is harder to extract heat away from the device. Secondly, GaAs is mechanically weaker than Si, this makes it much harder to produce large wafers which are needed for power electronics. Thirdly, there is no native oxide available in GaAs which makes it difficult to make more complex devices with insulated gate structures. Furthermore, GaAs has very low carrier lifetimes which limits the effectiveness of conductivity modulation in bipolar based power devices. Therefore, there has been no data regarding the cryogenic behaviour of power electronics based on GaAs. The only available data are for low power JFETs [54] and metal semiconductor field effect transistors (MESFETs) [55] [56].

SiC is a Si and carbon compound used in numerous applications from jewelry to nuclear fission fuel materials. It has also been found in LEDs and more recently power devices. The material exists in hundreds of polytype forms but in recent years, there has been huge interests in the semiconducting behaviour of three types of SiC for high power electronic applications. The polytypes are: 3C, 4H and 6H. SiC, as a power device material is superior to Si in many respects. It has one of the highest values of thermal conductivity amongst all the semiconductor materials. It is also an extremely hard material, at 9 - 9.5 on the Mohs scale compared to 10 for diamonds (the hardest materials) and 6.5 for Si, which makes it mechanically tough. SiC is a wide energy band-gap material with a bandgap of 2.4 - 3.2 eV

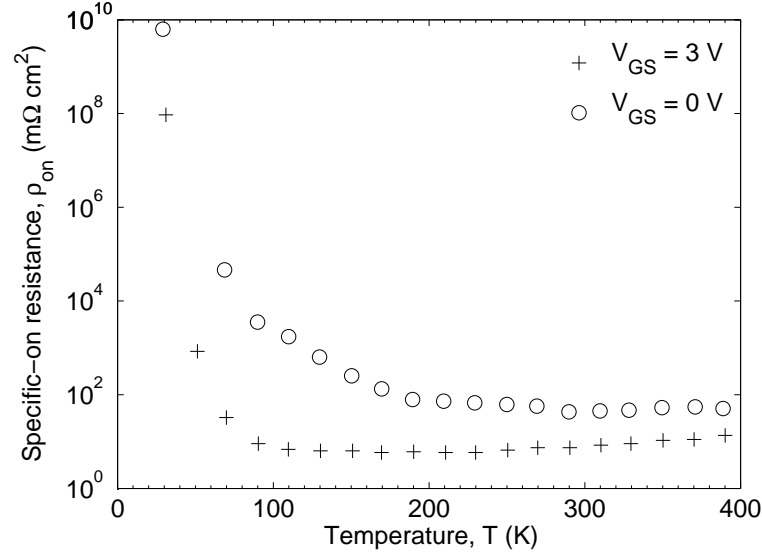


Figure 2.32: Temperature dependent specific-on resistance,  $\rho_{on}$  of a SiC vertical JFET (600 V, 3 A) at  $V_{GS}=0, 3$  V, measured by Cheng et al. [57].

(much higher than Si), making it an excellent material for high temperature operation. The critical electric field for SiC is an order of magnitude higher than Si, meaning a much thinner layer of SiC is required to sustain the same voltage compared to Si. This property is very attractive in power devices since it means SiC can operate at voltages/temperatures far beyond those that Si is capable of. It is also the only compound semiconductor that can be thermally oxidised, however the currently achievable oxide quality is relatively low compared to Si. There is a substantial amount of literature on SiC power devices, a large range of devices from Schottky diodes to power MOSFETs have been fabricated and tested in research. However, commercially available SiC devices are scarce and mainly focused on Schottky diodes and JFETs devices.

SiC are known to experiences carrier freeze-out at room temperatures, this is largely due to the high dopant ionisation energy of the associated dopants [58]. However, several studies have shown that SiC can be operated at cryogenic temperatures, 4H-SiC Schottky diodes down to 77 K [59] and recently for space application down to 103 K [60]. The cryogenic behaviour of a 4H-SiC vertical JFET (600 V, 3 A) was also measured down to 30 K by Cheng et al. [57], their measured specific on-state resistance at two different gate voltages

are shown in Fig. 2.32. The specific on-state resistance was shown to increase by several orders of magnitude at temperatures below 100 K due to carrier freeze-out effect. They also found the forward current peaks at  $\sim 225$  K and decreases at lower temperatures.

GaN is a III/V semiconductor with an energy band-gap even higher than SiC. Intrinsic GaN has a similar mobility to Si but with higher critical electric field compared to SiC. GaN is also a very hard material and can operate at high temperatures. However, its thermal conductivity is lower than that of Si and it has a fairly poor p-type with high dopant ionisation energy. It is also difficult and expensive to grow bulk GaN, however it is more common to grow epitaxial gallium nitride on other material substrates such as Si, sapphire and SiC. Due to this, it is uncommon to find a vertical device in GaN.

GaN has already been widely used in optoelectronic applications, such as LEDs and lasers. In recent years, there has been much interest in the high power capability of the GaN high electron mobility transistor (HEMT). Unlike doped semiconductors, where free carriers are generated by the number of dopants in the crystal lattice (see Chapter 3.1), a HEMT conducts via a two dimensional (2D) electron gas layer generated between the hetero-junctions. These hetero-junctions are normally between a wide band-gap highly doped n-type layer and an intrinsic narrow band-gap layer. When the two layers meet, all the electrons from the highly doped layer drop into the intrinsic layer to form the 2D electron gas layer. Since the electron layer is within the intrinsic semiconductor, the electron mobility can be extremely high (see Chapter 3.2). The aluminium gallium nitride/gallium nitride (AlGaN/GaN) used in GaN HEMT devices has additional carriers from the effects of spontaneous polarisation and piezoelectric polarisation, resulting in higher current capability [61]. Furthermore, the 2D electron gas density was found to be independent of temperature even down to cryogenic temperatures [62]. The basic structure of the AlGaN/GaN HEMT is presented in Fig. 2.33, the figure illustrates the location of the 2D electron gas layer that can be controlled by the gate terminal. This structure is for a normally on device. However, the HEMT device can be modified in a number of ways to become a normally off device as well.

Various studies have looked into the cryogenic behaviour of the low power GaN HEMT for RF applications, however no studies have been found which investigate the cryogenic

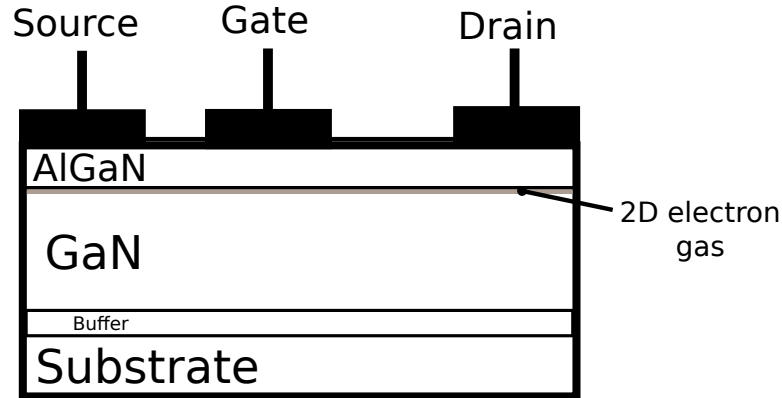


Figure 2.33: The basic HEMT device structure.

behaviour of high power GaN HEMT devices.

### 2.3.3 Discussion

Although Si based power electronics can operate at cryogenic temperatures, there are still some inherited problems due to the limitations of Si itself. Therefore, it is important to look beyond Si for materials that have superior properties. Table. 2.1 presents the figure of merit for all the semiconductor materials discussed in this chapter with the exception of SiGe which has properties between Si and Ge depending on the ratio of Si to Ge in the crystal. The table compares the intrinsic values of the discussed semiconductors, the boldface parameters highlight the most desirable values for the intended free-wheeling application and the underlined parameters shown the most undesirable. It should be noted that none of the most desirable values are within the Si column which means Si may not be the optimal material. However, none of the least desirable properties are found in Si either.

Theoretically, Ge and SiGe have some excellent characteristics, especially conductivity at cryogenic temperatures. The Ge and SiGe device measurements presented in this chapter have shown weak temperature dependence for the resistivity of materials and their diode threshold voltages are still relatively low at cryogenic temperatures. However, they lack good reverse breakdown capability and overall, they will never be better than Si in sustaining higher voltages. Also, they have low thermal conductivity and are mechanically weaker than

## 2.3 Introduction to Semiconductors Beyond Silicon

Table 2.1: Figure of merit for the semiconductors discussed in this chapter [63], the boldface parameters indicate the most desirable properties and the underlined parameters indicate the least desirable.

Parameter	Si	Ge	GaAs	SiC	GaN
Energy band-gap, $E_G$ @ 300 K (eV)	1.12	0.661	1.424	2.41 - 3.23	3.2
Critical electric field, $\mathbb{E}_c$ (V/cm)	$3 \times 10^5$	<u><math>1 \times 10^5</math></u>	$4 \times 10^5$	$1 - 3 \times 10^6$	<b><math>5 \times 10^6</math></b>
Electron mobility, $\mu_n$ ( $cm^{-2}/Vs$ )	$\leq 1400$	$\leq 3900$	$\leq$ <b>8500</b>	<u>400 - 900</u>	$\leq 1000$
Hole mobility, $\mu_h$ ( $cm^{-2}/Vs$ )	$\leq 450$	$\leq$ <b>1900</b>	$\leq 400$	<u>90 - 320</u>	$\leq 350$
Thermal conductivity, $K$ (W/Kcm)	1.3	0.58	<u>0.55</u>	<b>3.6 - 4.9</b>	1.3
Surface micro-hardness, $HK$ (kg/mm <sup>2</sup> )	1150	780	<u>750</u>	<b>2900 - 3100</b>	1200-1700

Si. This could be problematic if devices are scaled up for high power applications.

GaAs is an interesting material since it has the highest electron mobility at room temperature compared to any of other semiconductors discussed in this chapter. It also has a higher critical electric field than Si. However, it is not found in the power electronics industry due to its low thermal conductivity and mechanically weak wafers. Therefore, it would be difficult to obtain GaAs power devices for cryogenic measurements.

The thermo-mechanical properties of SiC are the most desirable. It has very high thermal conductivity and its hardness is comparable to diamond. The critical electric field is an order of magnitude higher than Si. It is an emerging power device material and SiC power MOSFETs are currently becoming commercially available. The only disadvantage is the low charge carrier mobilities, however, the presented measurements have shown that the specific-on resistance could improve at lower temperatures. Further investigation is required into the cryogenic behaviour of SiC devices.

GaN has the highest critical electric field of the materials in Table. 2.1, it is also mechanically tougher than Si and has similar thermal conductivity. However, unlike SiC the electron mobility is comparable to Si. Furthermore, the electron mobility of the 2D electron gas layer in the GaN HEMT is far above that of Si or SiC. This could result in a power device that has the ideal properties of both high breakdown voltage and low on-state resistance. Therefore, GaN has the potential to be the optimal material for cryogenic operations.

# An Introduction to Semiconductors Physics at Cryogenic Temperatures

The previous chapter introduced the various power devices and their known cryogenic behaviour. It was concluded that unipolar devices and especially the silicon power MOSFETs are the best candidate power device for cryogenic application. This chapter will introduce the known physics of silicon based electronics at cryogenic temperatures, including the various physical effects that contribute towards the overall cryogenic behaviour of unipolar power devices.

## 3.1 Introduction to Silicon

### 3.1.1 Energy Band Gap

As a semiconductor, silicon has a forbidden energy gap where energy states do not exist. Above this gap, the states are known as conduction band ( $E_C$ ) and the states below the gap are known as the valence band ( $E_V$ ), the energy separation between these two bands is known as the energy band gap ( $E_g$ ). The energy band gap is generally accepted to be over 1.12 electron volts (eV) at 300 K and approaches 1.17 eV at 0 K. The temperatures dependence of the energy band gap is shown in Fig. 3.1. The figure presents the various models and measured data on the subject. Macfarlane et al.'s measurements have indicated the energy band gap to be lower than 1.12 eV at room temperature [64], however more

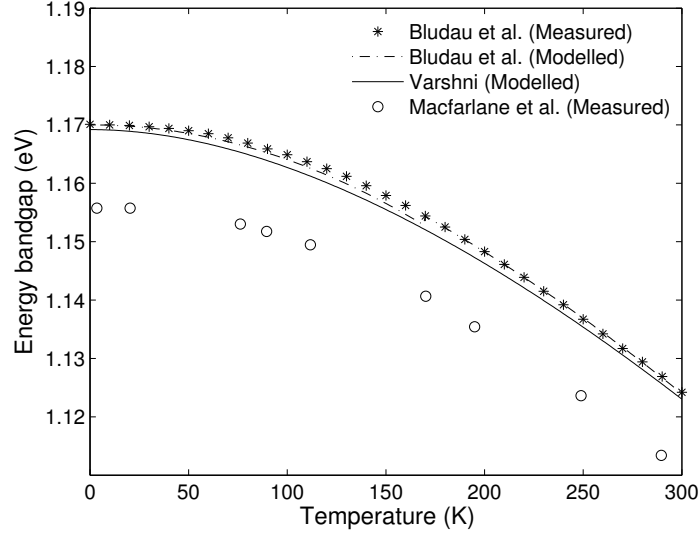


Figure 3.1: Various models and measured data on the energy band gap of silicon with temperature. Bludau et al. [65], Varshni [66] and Macfarlane et al. [64].

recent measurements from Bludau et al have indicated otherwise [65]. The energy band gap increases as temperature decreases, this has a significant effect on the behaviour of silicon power devices at cryogenic temperatures. The generally accepted temperature dependent model for the energy band gap is the Varshni equation [66]:

$$E_g(T) = E_0 - \frac{aT^2}{T + b}. \quad (3.1)$$

where  $E_0$  is the energy band gap at 0 K,  $a$  and  $b$  are constants. Alex et al. have given the constants as:  $E_0 = 1.1692$  eV,  $a = 4.9 \pm 0.2 \times 10^{-4}$  eV/K and  $b = 655 \pm 40$  K [67]. As shown in Fig. 3.1, the Varshni equation correlates with the data measured by Bludau et al. [65].

### 3.1.2 Intrinsic Silicon

The conductivity of silicon depends on the free carrier concentration of electrons in the conduction band and holes in the valence band. Electrons are fundamental particles which have a negative charge and are required to form the four covalent bonds in silicon crystal structures. Electrical current is conducted by electrons (liberated from broken bonds) moving

along in the conduction band in silicon. Holes are the absence of electrons in the covalent bonds and can be thought of as positively charged particles. They can appear to move along in the valence band as electrons jump from filled holes to unfilled holes. For intrinsic silicon the number of electrons in the conduction band and the number of holes in valence band should be equal as electrons in the conduction band have to be thermally excited from the valence band leaving an equal number of holes behind. The available excitation energy depends on the temperature. At thermal equilibrium, the net result is  $n = p = n_i$ , where  $n$  is the number of free electrons,  $p$  is the number of free holes and  $n_i$  is the intrinsic carrier concentration.

The temperature dependence of the intrinsic carrier concentration has been analysed by Caiafa et al. [68] and is presented in Fig. 3.2(a). They proposed the following model based on previous work by Barber [69]:

$$n_i = 4.81 \times 10^{15} \left( \frac{m_n^* m_p^*}{m_o^2} \right)^{0.75} T^{1.5} \exp\left(\frac{-E_g}{2kT}\right). \quad (3.2)$$

Here  $m_n^*$  and  $m_p^*$  are the electron and hole effective masses respectively,  $m_o$  is the electron rest mass and  $k_B$  is the Boltzman constant. In general, the electron/hole effective mass is a tensorial quantity which depends on the orientation of the crystal and this changes with temperature. The temperature variation is mainly due to the changes in the lattice spacing and Fermi distribution function. Caiada et al. also provided the temperature dependence of  $m_n^*$  and  $m_p^*$  in Eqn. 3.3 and 3.2(b) which are polynomial regression fits to the data measured by Barber [69]. This is shown in Fig. 3.2(b).

$$m_n^* = (-1.084 \times 10^{-9}T^3 + 7.580 \times 10^{-7}T^2 + 2.862 \times 10^{-4}T + 1.057)m_o, \quad (3.3)$$

$$m_p^* = (1.872 \times 10^{-11}T^4 + 1.969 \times 10^{-8}T^3 + 5.857 \times 10^{-6}T^2 + 2.712 \times 10^{-4}T + 0.574)m_o. \quad (3.4)$$

The shape of the intrinsic carrier concentration curve in Fig. 3.2(a) is mainly due to exponential function of the  $(-E_g/2kT)$  in Eqn. 3.2, which means  $n_i$  is highly dependent on the temperature variation of  $E_g$  and  $T$ . At room temperature the intrinsic carrier concentration is approximately  $1 \times 10^{10} \text{ cm}^{-3}$ . However, this decreases by ten orders of magnitude at



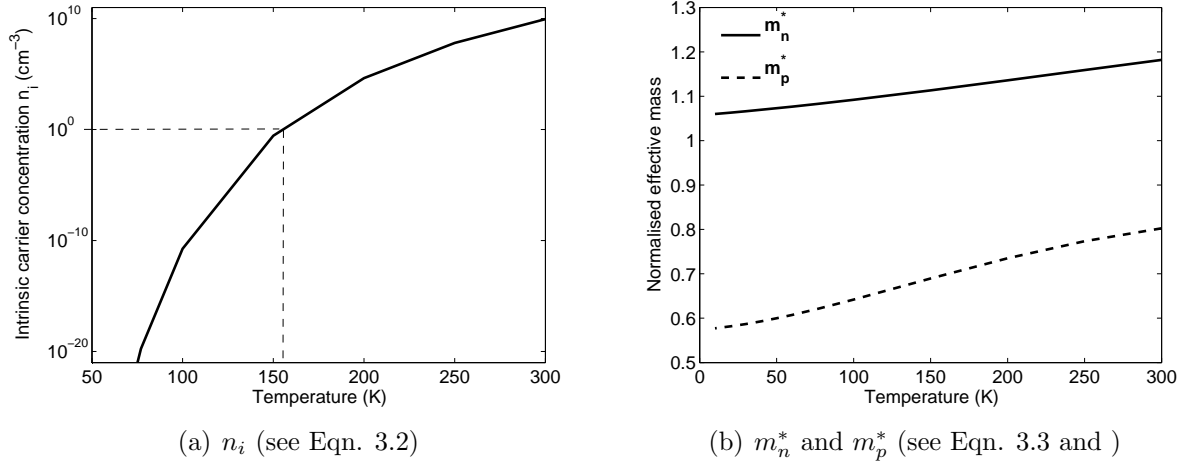


Figure 3.2: The temperature dependence of (a) the intrinsic carrier concentration and (b) the effective mass of electrons and holes, as modelled by Caiafa et al. [68].

$\sim 160$  K. Below this temperature, the intrinsic carrier concentration is so small that it can be considered negligible and no longer contributes towards the free carrier concentration.

### 3.1.3 Extrinsic Silicon

For intrinsic silicon, the free carrier concentration at room temperature is far too low to make it an effective semiconductor material. Therefore silicon is generally doped with other elements (dopants) to increase the free carrier concentration by several orders of magnitude in order to improve conductivity. Dopants are impurities within the silicon crystal lattice, they can be n-type (donors) or p-type (acceptors). The type indicates whether the dopant uses electronics (n-type) or holes (p-type) as its majority charge carrier. Donors have energy levels that sit within the silicon energy band gap, close to the conduction band. They are elements that have one or more extra electrons that are loosely bound to their dopant site. The electrons can be elevated to the conduction band with thermal excitation. The amount of energy required for this is called the ionisation energy. As the name suggests, acceptors are dopants that accept electrons rather than donate them. It can be said, therefore that they generate holes. Their energy levels are at the bottom of the silicon energy band gap, close to the valence band. They are elements that have one or more vacancies of electrons

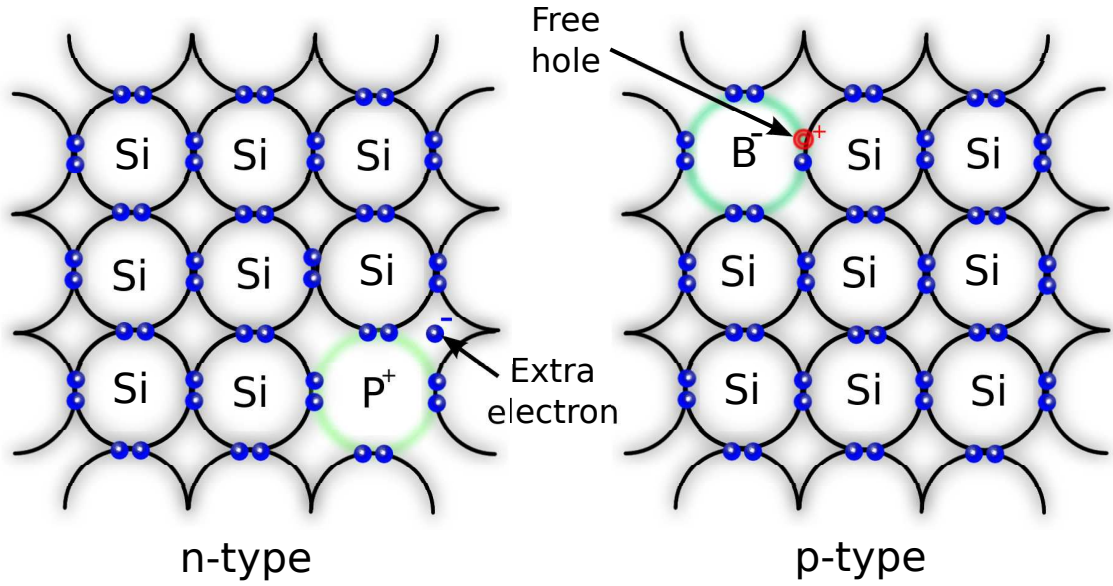


Figure 3.3: Bond pictures of n-type silicon doped with phosphorus and p-type silicon doped with boron.

when substituting a normal silicon atom within the covalent bond of the crystal lattice. It is important to note that when the doped crystal is depleted of carriers, the dopants are ionised with the opposite charge to their majority carriers. These ions form a potential barrier within the silicon lattice. There are several possible dopant types, the most common n-types are phosphorus (P) and arsenic (As) and for p-type, they are boron (B) and aluminium (Al). Fig. 3.3 illustrates the lattice structure of n-type silicon doped with P and p-type silicon doped with B.

Other than dopant types, the quantity of the additional impurity atoms can also alter the electrical properties of silicon. N-type silicon generally has a dopant concentration between  $10^{15} - 10^{18} \text{ cm}^{-3}$ . Lightly doped n-type silicon is normally denoted as  $n-$  and has a dopant concentration between  $10^{13} - 10^{14} \text{ cm}^{-3}$ . This is generally used in the drift region of high power devices. Highly doped silicon is denoted as  $n+$  and has a dopant concentration higher than  $10^{18} \text{ cm}^{-3}$ . The denotation of dopant concentration is the same for p-type silicon. Highly doped silicon ( $> 10^{18} \text{ cm}^{-3}$ ) is considered degenerate, this means that their behaviour is closer to metal than semiconductor. This is because with the high impurity concentration, the individual dopant atoms are close enough to form an impurity band which merges with

the conduction band and give rise to band gap narrowing effect.

## 3.2 Conductivity of Silicon

The conductivity ( $\sigma$ ) of silicon is greatly affected by temperature changes. It is expressed as:

$$\sigma = \frac{1}{\rho} = q(n(T, N_D)\mu_n(T, N_D) + p(T, N_A)\mu_p(T, N_A)). \quad (3.5)$$

where  $\rho$  is the resistivity,  $N_D$  is the donor concentration,  $N_A$  is the acceptor concentration,  $\mu_n$  is the electron mobility and  $\mu_p$  is the hole mobility. For purely n-type silicon, the conductivity simply becomes:

$$\sigma = qn(T, N_D)\mu_n(T, N_D). \quad (3.6)$$

Therefore, the change in conductivity with temperature will depend on free carrier concentration ( $n$ ) and electron mobility ( $\mu_n$ ).

### 3.2.1 Free Carrier Concentration

The number of charge carriers in a semiconductor is generally much lower than in a conductor. For intrinsic silicon, the free carrier concentration is approximately equal to  $n_i$ , see Fig. 3.4(a). However, with added impurities, the free carrier concentration would be approximately equal to the dopant concentration, see Fig. 3.4(b & c). Since at room temperature, the dopant concentration is generally several orders of magnitude higher than  $n_i$  and would therefore, dominate. For the rest of this chapter, only n-type silicon will be discussed in order to simplify the ideas. However, equivalent equations and discussions can be applied to p-type silicon.

#### 3.2.1.1 Effects of Temperature on Electron Concentration

Fig. 3.5 presents the temperature dependence of  $n$  for n-type silicon with a dopant concentration of  $1 \times 10^{15} \text{ cm}^{-3}$  [70]. The figure illustrates the three temperature regions of operation for silicon. Silicon normally operates in the saturation region where all the donors are ionised

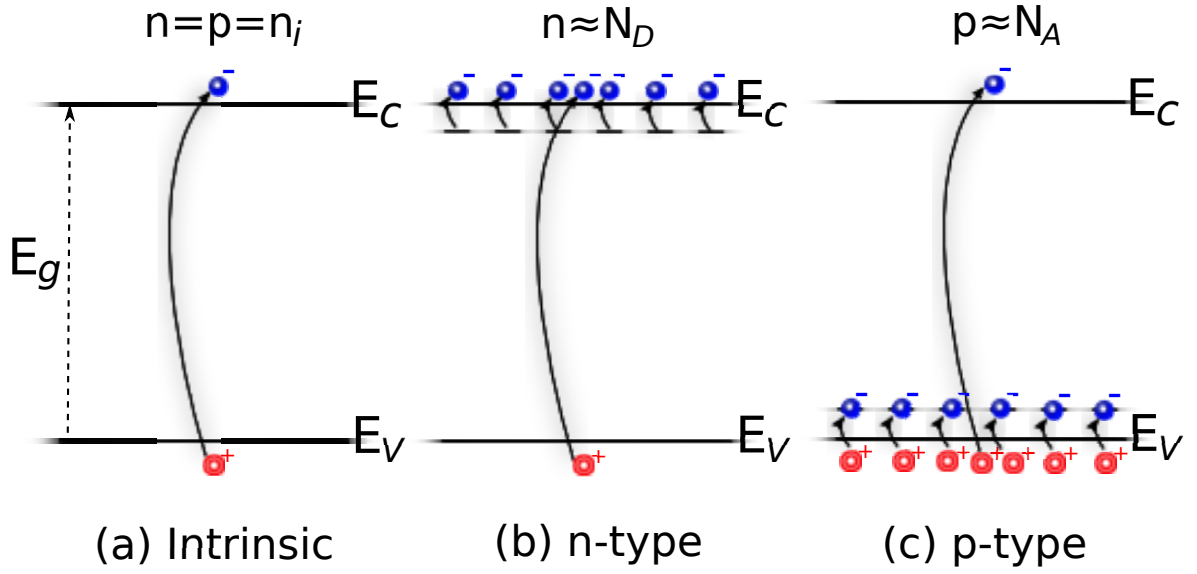


Figure 3.4: The contribution to the free carrier concentration for (a) intrinsic silicon, (b) n-type silicon and (c) p-type silicon.

and  $N_D \approx n$ . At high temperature conditions, silicon enters the intrinsic region where the intrinsic carrier concentration becomes higher than the dopant concentration,  $n_i > N_D$  and  $n \approx n_i$ . This is when the thermal energy inside the silicon is high enough to excite the electrons from the valence band to the conduction band and the electrons available from the silicon crystal lattice is much higher than the dopant concentration. In this region, silicon no longer behaves like a semiconductor due to the high leakage current, hence it is the upper limit of the operating temperature. At cryogenic temperatures, silicon enters the freeze-out range where there is not enough thermal energy to ionise all the donors and incomplete ionisation takes place, where  $n < N_D$ .  $n$  can be approximated by [71]:

$$n \approx \sqrt{\frac{N_D N_C}{2}} \exp\left(-\frac{qE_i}{2kT}\right), \quad (3.7)$$

here  $E_i$  is the ionisation energy and is equal to  $E_C - E_D$ , where  $E_D$  is the donor energy level.  $E_i$  varies with different impurity types, Table 3.1 presents some of the common dopant species and the values of their  $E_i$ . The most common n-type dopant for silicon is phosphorus where  $E_i \approx 46 \text{ meV}$ .  $E_i$  is a critical parameter for any semiconductor since a low value reduces the

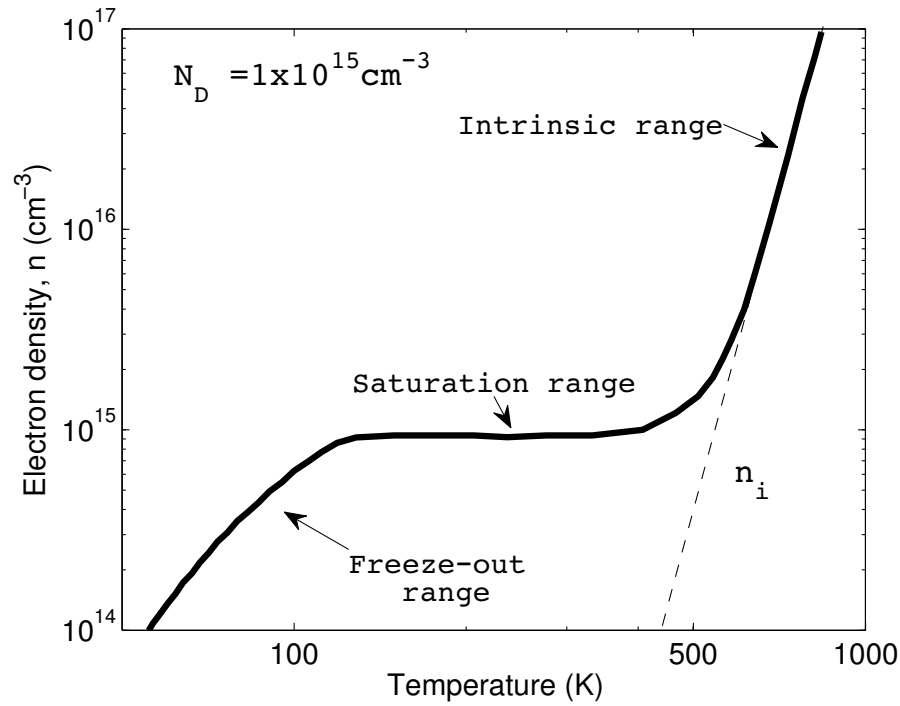


Figure 3.5: The free electron concentration as a function of temperature for silicon with  $N_D = 1 \times 10^{15} \text{ cm}^{-3}$  [70].

carrier freeze-out temperature. However, a high value of  $E_i$  causes freeze-out to occur even at room temperatures. Fig. 3.6 shows a more complete picture of the freeze-out range of silicon [72], the freeze out range can be further separated into transition range and insulator range. The transition range sits between the saturation range and the insulator range. Incomplete ionisation occurs in the transition range. Here the thermal energy of the crystal lattice is not high enough to ionise all the donors and a fraction of the electrons occupy the donor sites instead of the conduction band.  $n$  is highly dependent on  $T$  in this temperature range. The insulator range is where the carrier freeze-out is complete and all the electrons are frozen to the donor sites and  $n$  becomes virtually zero.

### 3.2.1.2 Effects of Dopant Concentration on Electron Concentration

At room temperature incomplete ionisation can still occur [73]. At higher dopant concentrations the thermal energy of the crystal may not be enough to completely ionise all the

Table 3.1: Various impurities used in N and P-type silicon and their ionisation energy,  $E_i$  [61]

N-type dopants species	$E_i$ (meV)	P-type dopants species	$E_i$ (meV)
P	46	B	44
As	54	Ga	73
N	190	Al	69

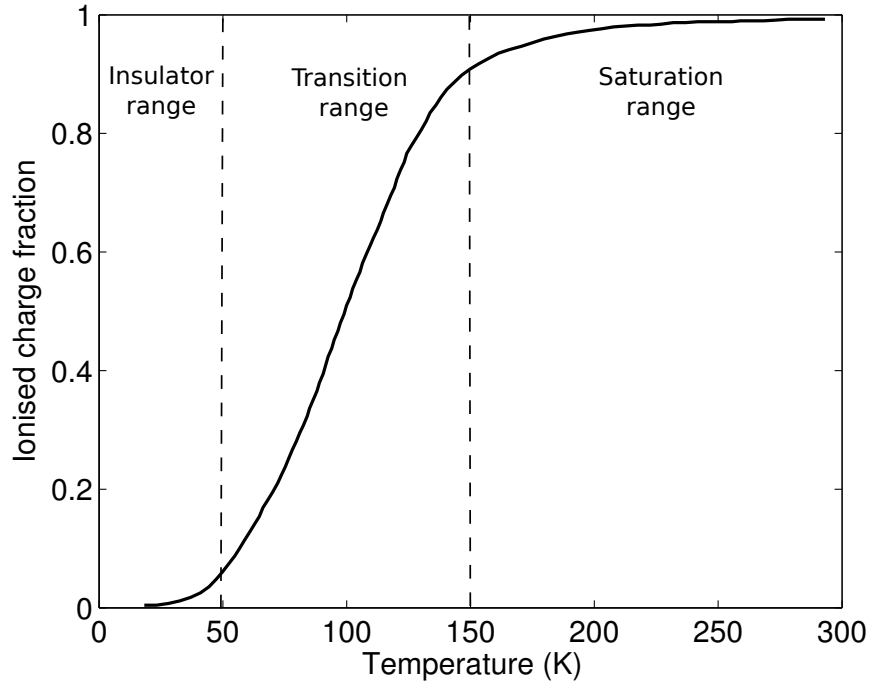


Figure 3.6: The ionised charge fraction of n-type silicon (phosphorus) against temperature for dopant concentration  $1 \times 10^{15} \text{ cm}^{-3}$  [72].

donors and a fraction of the donors will remain un-ionised. Most physical models tend to neglect this effect or assume incomplete ionisation becomes more severe at very high  $N_D$ . In fact, at room temperature, only a narrow band of dopant concentrations are affected by incomplete ionisation. An empirical model was published by Schenk et al [73], where the ionised charge fraction is given by:

$$\frac{N_D^+}{N_D} = 1 - \frac{bn}{(n + gn_1)}. \quad (3.8)$$

Here  $N_D^+$  is the ionised dopant concentration and  $b$  is a doping dependent attenuation factor given as:

$$b = \frac{1}{1 + (N_D/N_b)^d}, \quad (3.9)$$

$n_1$  is given as:

$$n_1 = N_C \exp\left(-\frac{qE_{dop}}{kT}\right), \quad (3.10)$$

and  $E_{dop}$  is given as:

$$E_{dop} = \frac{E_i}{1 + (N_D/N_{ref})^C}. \quad (3.11)$$

Other parameters are given in Table 3.2 with phosphorus as the dopant. Fig. 3.7 illustrates the incomplete ionisation effect of Eq. 3.8 at 300 K for silicon doped with phosphorus at various concentrations. The figure shows complete ionisation when  $N_D \leq 1 \times 10^{16} \text{ cm}^{-3}$  and  $N_D \geq 1 \times 10^{20} \text{ cm}^{-3}$ . The fraction of ionised dopants drops to 75% when  $N_D$  is around  $3 \times 10^{18} \text{ cm}^{-3}$ . The reason for the complete ionisation for low dopant concentrations is due to the silicon operating in the saturation region, as shown in Fig. 3.5. Complete ionisation at ultra high dopant concentrations is due to the degeneracy of silicon. This is where impurity energy band width becomes wide enough to merge with the conduction band edge, commonly known as the Mott transition [74]. Once  $N_D$  is high enough to pass the Mott transition point, dopant ionisation becomes temperature independent even at cryogenic temperatures.

The incomplete ionisation effect is also dependent on temperature. At lower temperatures, less thermal energy will become available to ionise all the available dopants. Therefore silicon with a lower dopant concentration can still be affected by the incomplete ionisation effect. The narrow band of dopant concentration that is affected by incomplete ionisation at room temperature will become wider and the centre of the band will shift towards lower dopant concentrations, as shown on Fig. 3.7.

### 3.2.1.3 Effects of Electric Field on $n$

If thermal ionisation is the only mechanism to ionise dopants, silicon would behave like an insulator in the insulator temperature range. However, there are other ionisation mechanisms that depends on the electric field. Their effects are weak at room temperature, therefore they

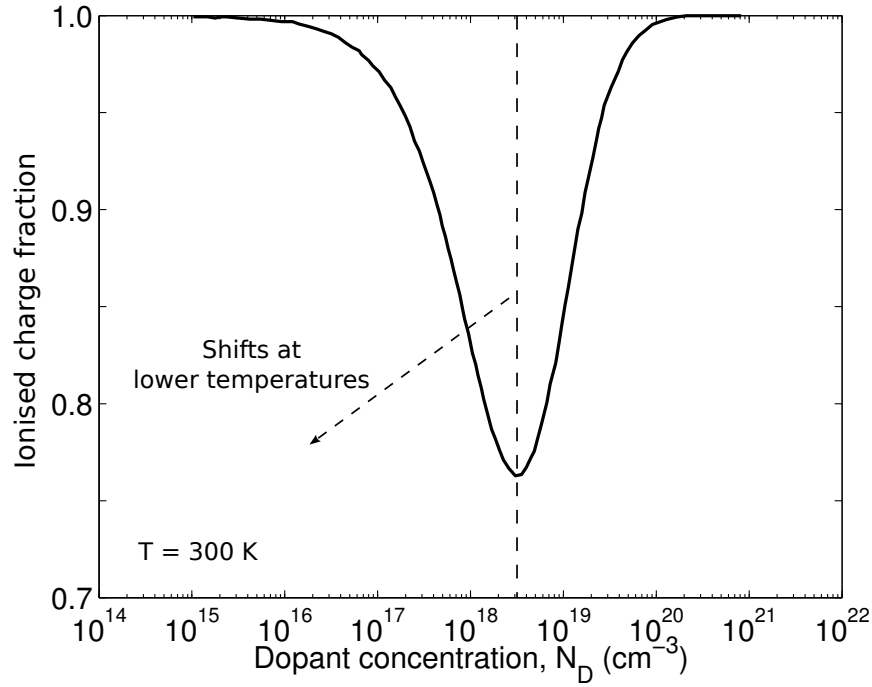


Figure 3.7: The ionised charge fraction of silicon doped with phosphorus at different concentration [73].

Table 3.2: Parameters used in Eq. (3.8), (3.9) and (3.11) for phosphorus

Parameter	Value
$N_{ref} [cm^{-3}]$	$2.2 \times 10^{18}$
$C$	2
$N_b [cm^{-3}]$	$6 \times 10^{18}$
$d$	2.3
$g$	0.5

are not generally noticeable. At low temperatures where the thermal ionisation mechanism becomes weaker than the electric field ionisation mechanisms, the electric field effects become dominant. For the temperature range of interest, two electric field dependent ionisation mechanisms are known, they are discussed below.



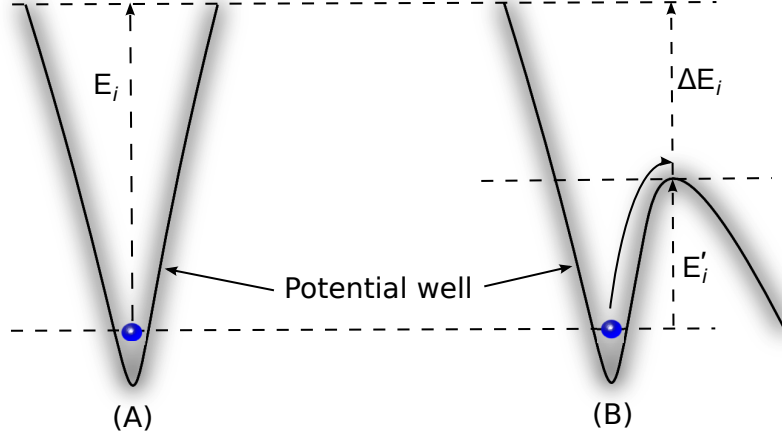


Figure 3.8: The potential well of a trapped electron at an un-ionised donor site with (A) no electric field presence and (B) with electric field and potential barrier bending.

#### 3.2.1.4 Poole-Frenkel Ionisation

For un-ionised donor sites, the trapped electron is in a funnel shaped potential well [75]. The height of the well is the ionisation energy that is required for the electron to be excited to the conduction band, see Fig. 3.8(A). However, the potential well can be bent by an electric field to a lower ionisation energy ( $E'_i$ ), see Fig. 3.8(B).  $\Delta E_i$  is the difference between  $E_i$  and  $E'_i$ , it is dependent on the electric field ( $\mathbb{E}$ ) [75]:

$$E'_i = (E_i - \Delta E_i) = E_i - 2q\sqrt{\frac{q\mathbb{E}}{\varepsilon_{si}\varepsilon_0}}. \quad (3.12)$$

Here  $\varepsilon_{si}$  is the dielectric constant of silicon and  $\varepsilon_0$  is the permittivity of vacuum. For silicon, the donors are already ionised at room temperature through the thermal mechanism. Therefore, the Poole-Frenkel effect is not easily noticeable. It becomes noticeable at carrier freeze-out temperatures ( $<50$  K). Even though Poole-Frenkel ionisation is an electric field effect, the actual ionisation mechanism is still based on thermal excitation. Therefore this effect is also known as field-assisted thermal ionisation.

### 3.2.1.5 Tunnelling Ionisation

Other than Poole-Frenkel ionisation, tunnelling is also a possible ionisation mechanism. However, unlike Poole-Frenkel ionisation, tunnelling is a form of field induced ionisation which is only weakly dependent on temperature. If the electric field strength is sufficiently high an electron can tunnel through the lowered barrier side of the potential well into the conduction band, see Fig. 3.9 [75]. This requires no thermal ionisation and could operate at near zero kelvin temperatures. Therefore, tunnelling dominates at temperatures below 10 K where Poole-Frenkel effects are minimal.

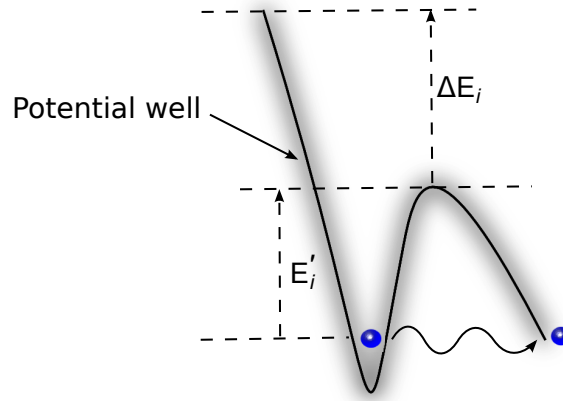


Figure 3.9: Tunnelling effect - when an electron tunnel through the lowered barrier side of the potential well.

### 3.2.2 Electron and Hole Mobilities

The electron and hole mobilities ( $\mu_n, \mu_p$ ) have direct influence over the conductivity of silicon at any given temperature. They quantitatively describe how charge carriers move through the silicon crystal and are directly related to the drift velocity ( $v_d$ ) caused by the presence of an electric field. They are defined as:

$$v_{d(n,p)} = \mu_{n,p} \mathbb{E}. \quad (3.13)$$

When an electric field is applied across a silicon crystal, the free charge carriers are accelerated by the electrical force and decelerated by collisions and lattice scattering events. The results are two average drift velocities that can be described by the variable  $\mu_{n,p}$ .

For n-type silicon,  $\mu_n$  can be approximated by the Matthiessen's rule where a combinations of scattering mechanisms are combined together:

$$\frac{1}{\mu_n} = \frac{1}{\mu_L} + \frac{1}{\mu_i} + \frac{1}{\mu_{eh}} + \frac{1}{\mu_{ee}}. \quad (3.14)$$

$\mu_L$  is the lattice scattering effect, otherwise known as phonon scattering. This is due to the lattice vibrations which produce acoustic pressure waves/quasi-particles known as phonons. The energy and concentration of phonons are dependent on temperature and their collisions with moving electrons are the main factor in reducing  $\mu_n$ .  $\mu_i$  is the impurity scattering effect, caused by the collisions between electrons and the added impurities. The collision is caused by coulomb scattering due to the positively charged dopant ions.  $\mu_i$  is different for different dopant types and concentrations.  $\mu_{eh}$  is the electron and hole scattering process, this becomes significant at high temperatures where a large amount of holes are generated from the intrinsic carrier ionisation process which can cause coulomb scattering with the electrons.  $\mu_{ee}$  is the electron-electron scattering process, this becomes significant at very high electron density where the electrons spatial proximity becomes very small and the repulsive force between them increases the collisions with one another.

### 3.2.2.1 Effects of Dopant Concentration on Electron and Hole Mobilities

The electron and hole mobilities in bulk silicon can be affected by a number of controllable variables, such as the dopant concentration and temperature. Clearly, intrinsic silicon, which has little or no impurities would induce very little impurity scattering. Increasing the dopant concentration increases impurity scattering which results in lower electron mobility. High dopant concentrations increase the charge carrier concentration, which increases the coulomb

scattering processes, reducing the charge carrier mobilities. Fig. 3.10 shows the electron mobility as a function of dopant concentration. The function is based on Caughey and Thomas's empirical data [76]. The function is expressed as:

$$\mu_{n,p} = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (N_{D,A}/N_{ref,1})^{\alpha_1}}. \quad (3.15)$$

The coefficients are presented in Table 3.3 [77] for phosphorus and boron as the dopant species.

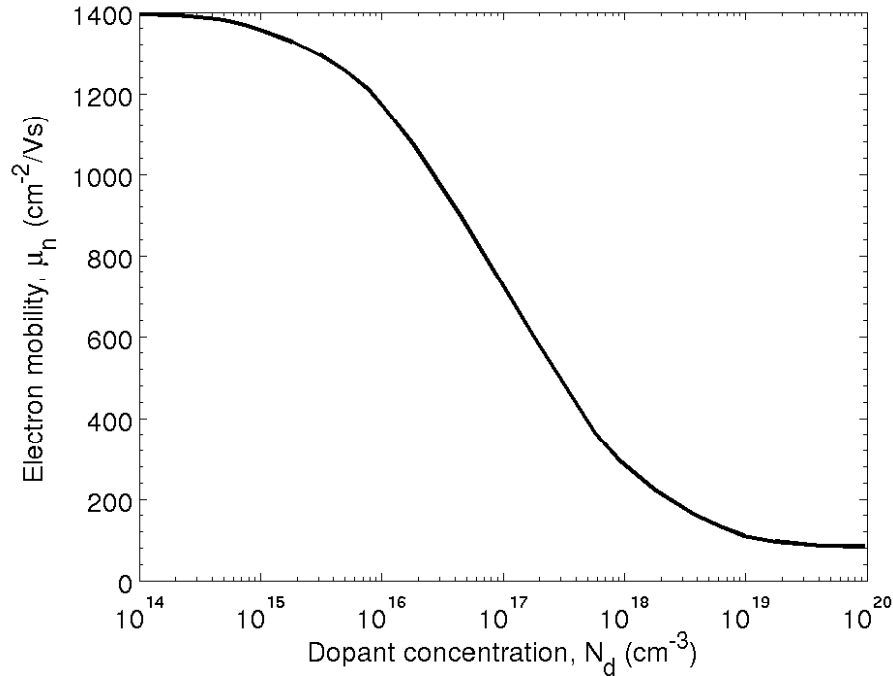


Figure 3.10: The electron mobility,  $\mu_n$  as a function of dopant concentration (phosphorus),  $N_D$  based on empirical data [76] (for low electric fields).

The figure shows that the electron mobility is unaffected by impurity scattering at dopant concentrations below  $1 \times 10^{14} \text{cm}^{-3}$  but becomes dependent as  $N_D$  increases. At very high dopant concentrations, the electron mobility appears to saturate at a constant value [78]. Further work by Masetti et al. has indicated that at dopant concentrations above  $1 \times 10^{20} \text{cm}^{-3}$ , the electron mobility saturates at a lower value than previously suggested [79]. This is shown in Fig. 3.11 where the dashed line indicates the expected electron mobility

Table 3.3: Coefficients used in Eq. (3.15), (3.16), (3.17) and (3.18) for phosphorus and boron as impurities.

Coefficients	P	B
$\mu_{max}(cm^2/Vs)$	1414.0	470.5
$\mu_{min}(cm^2/Vs)$	68.5	44.9
$\mu_1(cm^2/Vs)$	56.1	29.0
$N_{ref,1}(cm^{-3})$	$9.20 \times 10^{16}$	$2.23 \times 10^{17}$
$N_{ref,2}(cm^{-3})$	$3.41 \times 10^{20}$	$6.10 \times 10^{20}$
$\alpha_1$	0.711	0.719
$\alpha_2$	1.98	2.0

saturation and the solid line is based on empirical data. This behaviour can be included in Eqn. 3.15 to give Eqn. 3.16. The coefficients are presented in Table 3.3.

$$\mu_n = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (N_D/N_{ref,1})^{\alpha_1}} - \frac{\mu_1}{1 + (N_{ref,2}/N_D)^{\alpha_2}}, \quad (3.16)$$

### 3.2.2.2 Effects of Temperature on Electron and Hole Mobilities

As well as dopant concentration, charge carrier mobilities are also sensitive to temperature. At elevated temperatures, the carrier mobilities decrease due to high lattice scattering from electron/hole-phonon collision events, as well as increased coulomb scattering between both charge species due to increased free carrier concentration. When the lattice temperature is reduced, the behaviour is reversed. Phonons will have a lower average energy which will reduce the lattice scattering events, coulomb scattering will also diminish due to the lower free carrier concentration. However, carrier mobilities remain sensitive to impurity scattering which means it is always affected by the dopant concentration.

Fig. 3.12 presents a selection of previously measured electron and hole mobilities against temperature at different dopant concentrations. The figures show large increases in the electron and hole mobilities, especially at lower dopant concentrations. Fig. 3.12(a) shows that at conventional operating temperatures (250-350 K), silicon with very low dopant concen-

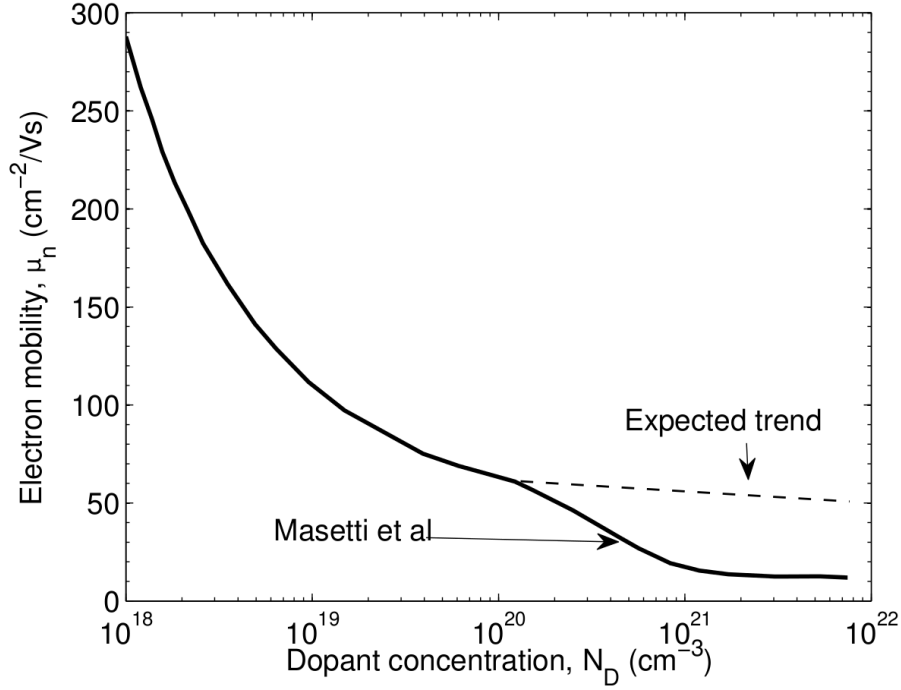


Figure 3.11: The electron mobility,  $\mu_n$  as a function of high dopant concentration. The solid line is based on empirical data [79].

trations ( $< 1 \times 10^{14} \text{cm}^{-3}$ ) follows the generally accepted  $T^{-2.42}$  dependence but deviates at higher dopant concentrations. Mobilities saturations were also observed at low temperatures and the saturation temperatures appear to be higher at higher dopant concentrations. For extremely low dopant concentrations ( $N_D < 10^{12} \text{cm}^{-3}$ ), the electron mobility at 10 K is three orders of magnitude higher than at 300 K with no observable saturation at any temperature. This suggests that coulomb scattering could be the cause for the saturation which occurs at low temperatures. For highly doped silicon ( $N_D \approx 1.3 \times 10^{17} \text{cm}^{-3}$ ), the electron mobility at 50 K is only one order of magnitude higher than at 300 K. Below 50 K, the electron mobility appears to decrease as temperature tends towards absolute zero, indicating a peak mobility at 50 K. The reason for the inverse temperature dependence in this temperature range is uncertain. At even higher dopant concentrations ( $N_D \geq 2.5 \times 10^{18} \text{cm}^{-3}$ ), the increase with decreasing temperature is minimal. This means the electron mobility is almost temperature independent around 300 K. For the hole mobilities shown in Fig. 3.12(b),

the temperature dependent behaviour at high dopant concentrations is relatively similar to the electron mobility. However, for extremely pure samples, the hole mobilities appear to increase monotonically at cryogenic temperatures.

Charge carrier mobilities are particularly difficult to model accurately since they are sensitive to several variables simultaneously. The two main variables have been discussed already: dopant concentration and temperature. For extreme temperature cases, one more variable should be included: the free carrier concentration. Klasseen presented a model which accounts for all three variables [77,81] and is based on Matthiessen's rule from Eqn. 3.14 where the temperature dependent lattice scattering effect is expressed as:

$$\mu_L = \mu_{max} \left( \frac{300}{T} \right)^{2.285}, \quad (3.17)$$

and impurity scattering which is also dependent on the free carrier concentration ( $n$ ) is expressed as:

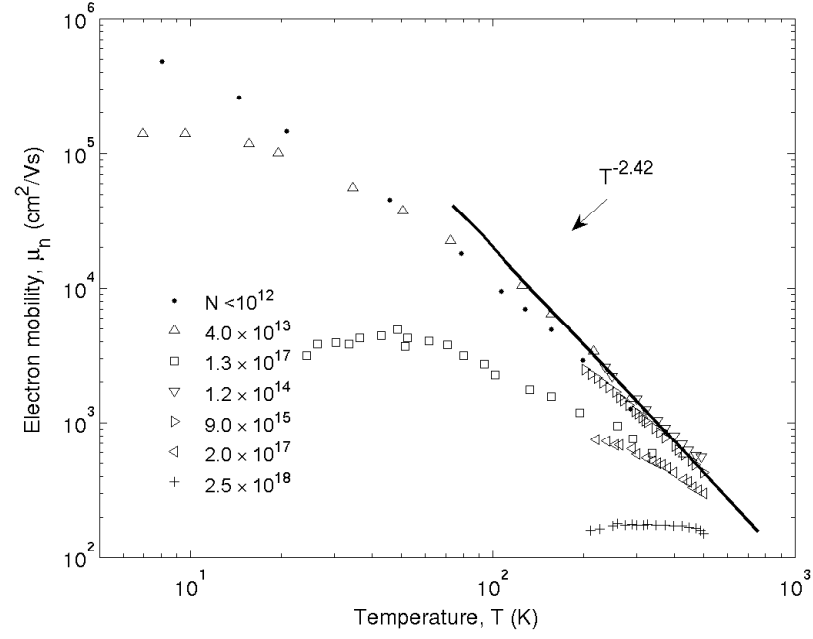
$$\mu_i = \frac{\mu_{max}^2}{\mu_{max} - \mu_{min}} \left( \frac{T}{300} \right)^{3\alpha_1 - 1.5} \left( \frac{N_{ref,1}}{N_D} \right)^{\alpha_1} + \frac{\mu_{min}\mu_{max}}{\mu_{max} - \mu_{min}} \left( \frac{300}{T} \right)^{0.5} \left( \frac{n}{N_{D,A}} \right). \quad (3.18)$$

Coefficients can be found in Table 3.3.

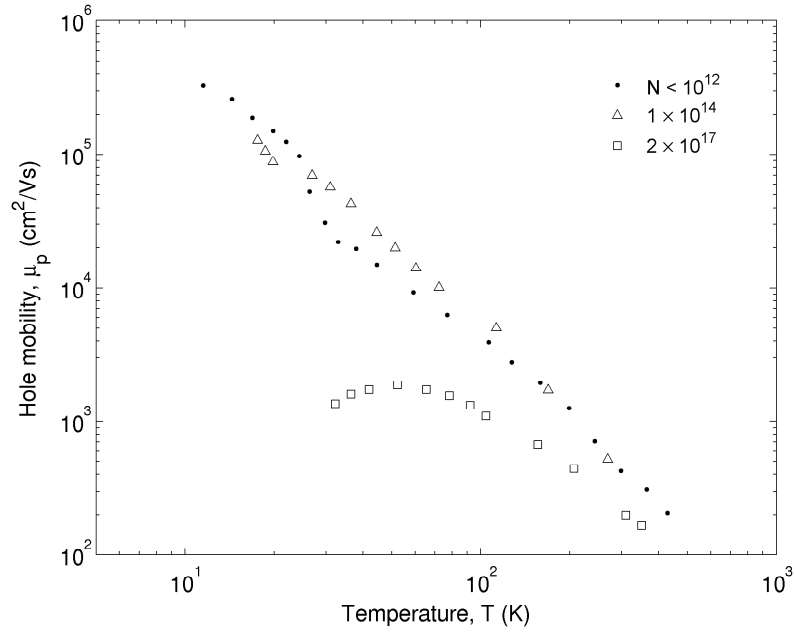
### 3.2.2.3 Saturation Velocity

All the previous discussions have assumed the charge carrier mobilities to be constant for all electric field conditions and that the electron and hole velocities would increase/decrease linearly in proportion to the electric field strength. However, at very high electric field conditions, carrier velocity cannot increase indefinitely and the mobility falls towards zero. The maximum velocity that can be reached is known as the saturation velocity. The saturation velocity at high electric field strengths is dependent on temperature, dopant concentration and crystallographic orientation.

Fig. 3.13(a) presents the temperature dependent electron drift velocities against electric field applied parallel to the  $\langle 111 \rangle$  crystallographic orientation [80]. At 20 K, the electron saturates at an electric field strength that is approximately an order of magnitude lower



(a) Electron mobilities



(b) Hole mobilities

Figure 3.12: Previously measured (a) electron mobilities and (b) hole mobility data as a function of temperature at different dopant concentrations.  $\bullet$ ,  $\triangle$  and  $\square$  were presented in [80].  $\nabla$ ,  $\triangleright$ ,  $\triangleleft$  and  $+$  were presented in [81]. The solid line illustrates the  $T^{-2.42}$  dependence for silicon with low dopant concentration.



than at 300 K. The saturation velocity increases further at lower temperatures, as shown in Fig. 3.13(b) based on empirical data presented in [80]. The curve follows the temperature dependent equation:

$$v_{sat}(T) = \frac{2.4 \times 10^7}{1 + 0.8 \exp(T/600)}. \quad (3.19)$$

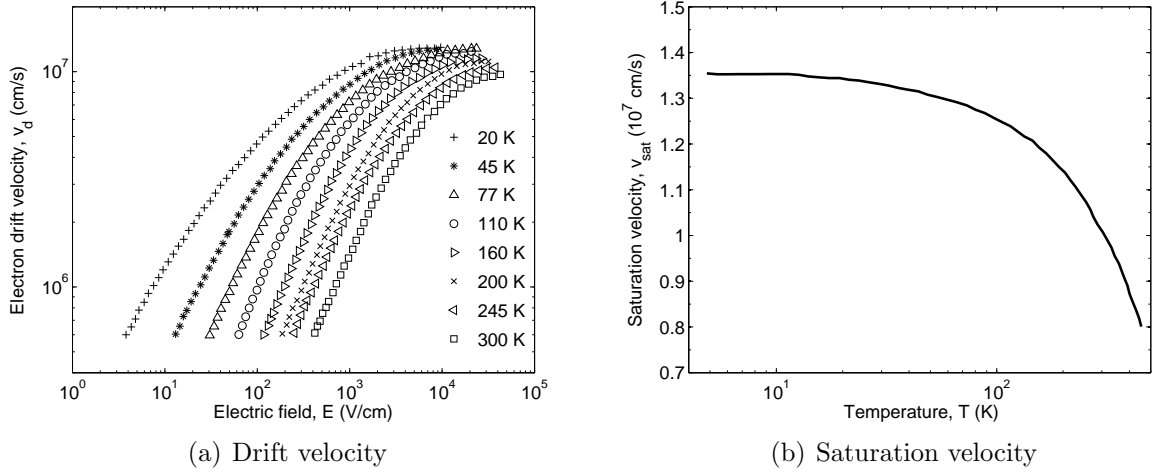


Figure 3.13: The temperature dependent (a) electron drift velocity against electric field applied parallel to the  $\langle 111 \rangle$  crystallographic orientation and (b) saturation velocity best fit curve from empirical data following Eqn. 3.19 [80].

### 3.2.2.4 Surface effects on the electron mobility

As discussed in the previous chapter, the metal-oxide-semiconductor (*MOS*) structure is critical in all MOS devices. The inversion channel resistance is a major contribution to the total on-state resistance. This is especially true for devices with blocking voltages below 100 V. This is because the electron mobility at the channel is lower than the bulk electron mobility we have discussed earlier in this section. The electrons are forced to travel through the thin inversion layer at the surface of the silicon. Here, they experience several other scattering effects that only occur at the oxide-semiconductor junction as well as the scattering effects electrons normally encounter in bulk silicon. These include additional coulomb scattering from the fixed oxide charges and interface state charges. Interface state charges come from the oxide surface, surface roughness scattering due to the surface mismatch and

oxide quality. The electron mobility is also directly affected by the applied electric field normal to the semiconductor surface and the background dopant concentration of the semiconductor, inversion layer charge density and crystallographic orientation. Various studies have concluded that the  $\langle 100 \rangle$  crystallographic orientation provides the best electron mobility, therefore manufacturers tend to use this orientation as the starting material in silicon devices [23].

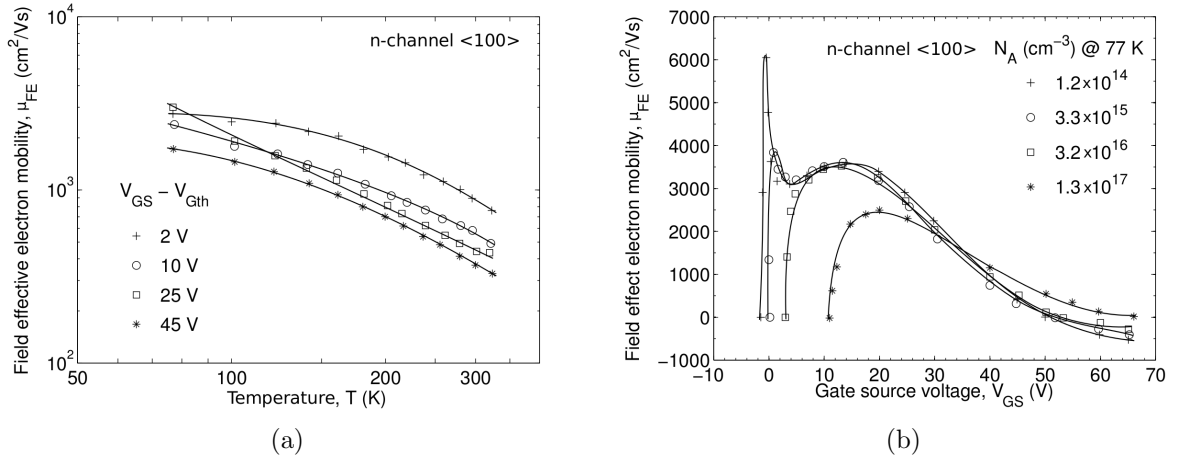


Figure 3.14: (a) The temperature dependent field effect electron mobilities and (b) the field effect electron mobilities at 77 K for different dopant concentration [82] for n-channel MOS with silicon crystallographic orientation ( $\langle 100 \rangle$ ).

The field effect electron mobility ( $\mu_{FE}$ ), effectively the inversion layer electron mobility, has been measured by Sato et al. [82] down to 77 K. Fig. 3.14(a) presents their measured temperature dependence at four different gate voltages for n-channel MOS gates with silicon in the  $\langle 100 \rangle$  crystallographic orientation. Down to 77 K, the electron mobility exhibits a monotonic increase, but decreases with higher gate voltages. Interestingly, at 77 K, the electron mobility at 25 V,  $V_{GS} - V_{Gth} > 2$  V indicating a possible peak electron mobility for  $10 \text{ V} < V_{GS} < 45 \text{ V}$ . This is confirmed in Fig. 3.14(b). The figure shows the electronic mobility behaves in a non-monotonic manner and peaks at  $\sim 15$  V for  $N_A = 3.2 \times 10^{16} \text{ cm}^{-3}$ . Increasing gate voltages leads to higher inversion layer charge density. Beyond a certain voltage, the carrier density becomes high enough to induce serious electron-electron scattering effects. Lower dopant concentrations have similar electron mobilities at high gate voltage

but do not lead to gate threshold voltages. Higher dopant concentrations reduce the electron mobility as well as increasing the gate threshold voltage.

A physical semi-empirical model that is accurate down to 77 K was proposed by Jeon and Burk [83], it accounts for scattering mechanisms including phonon, coulomb and surface roughness. For the temperatures between 100 K and 370 K, the inversion layer electron mobility can be modelled as:

$$\mu_{inv} = \frac{T}{a_1} + \frac{1}{a_2 T^n \mathbb{E}_{eff}^{1/\gamma}} + \frac{1}{a_3 \mathbb{E}_{eff}^2}, \quad (3.20)$$

and between 77 K and 100 K,

$$\mu_{inv} = \frac{\mathbb{E}_{eff}^\alpha}{a_4 T} + \frac{1}{a_5 T \mathbb{E}_{eff}^{1/3}} + \frac{1}{a_6 \mathbb{E}_{eff}^2}, \quad (3.21)$$

with the effective electric field in the inversion layer as:

$$\mathbb{E}_{eff} = \frac{1}{\varepsilon_0 \varepsilon_{si}} (0.5 Q_{inv} + Q_{depl}). \quad (3.22)$$

where  $Q_{inv}$  is the inversion layer carrier concentration and  $Q_{depl}$  is the depletion region charge density. All other parameters are presented in Table. 3.4.

Also affected by the surface effect is the accumulation layer mobility, which for a power MOSFET occurs in the n-type JFET (throat) region directly under the gate oxide. Compared to the number of studies on the inversion layer, relatively little works has been done on the cryogenic behaviour of the accumulation layer. However, Wilcox et al. [84] measured the behaviour down to 30 K at  $\mathbb{E}_{eff}=1 \times 10^5 V/cm$ . The data is presented in Fig. 3.15. The figure also includes the temperature dependent model of the accumulation mobility:

$$\mu_{accu} = 757 \left( \frac{T}{300} \right)^{-0.7}. \quad (3.23)$$

Table 3.4: Parameters used in Eqn. 3.20 and 3.21.

Parameters	Values
$a_1$	$6.68 \times 10^{-8}$
$a_2$	$1.82 \times 10^{-8}$
$a_3$	$3.27 \times 10^{-16}$
$a_3$	$6.38 \times 10^5$
$a_3$	$2.65 \times 10^{-8}$
$a_3$	$4.89 \times 10^{-16}$
$n$	1.62
$\gamma$	4.89
$\alpha$	2.04

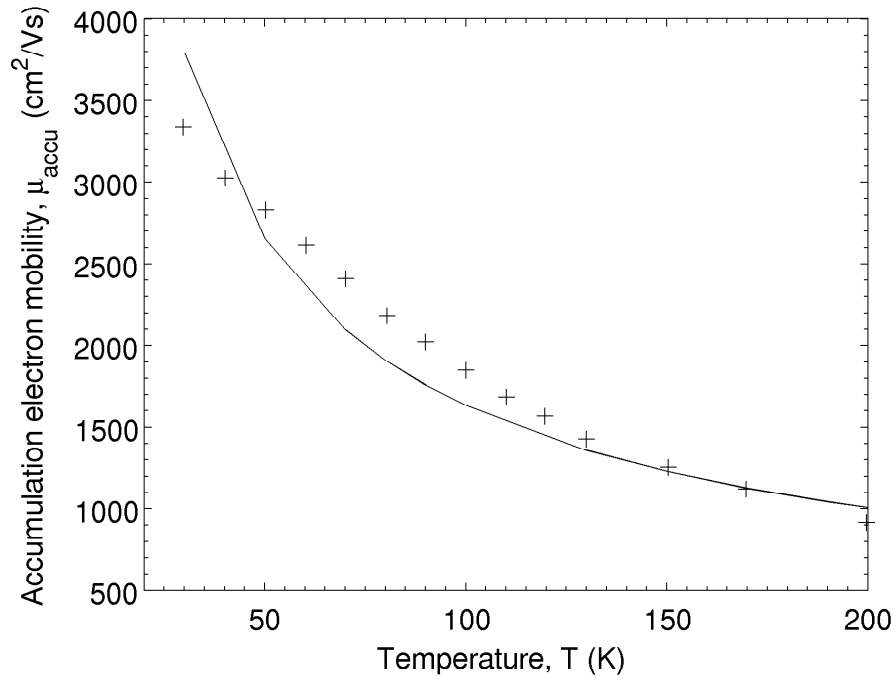


Figure 3.15: (+) The measured accumulation electron mobility at  $\mathbb{E}_{eff}=1 \times 10^5 V/cm$  [84] and the solid line represents the temperature dependent model in Eqn. 3.23.

### 3.3 Breakdown Behaviour

One of the key properties of power devices is the ability to support high blocking voltages, therefore understanding the breakdown mechanism in silicon is particularly important. All power devices have a rated breakdown voltage ( $V_{BD}$ ). Operating the device around the breakdown voltage should be avoided since the combined effects of high voltage and high current will lead to severe power dissipation. This would result in device degradation or even irreversible destruction.

There are several mechanisms that could lead to junction breakdown, by far the most common is impact ionisation. Other mechanisms, such as thermal instability (due to ultra high temperatures) are not applicable at cryogenic temperatures and tunnelling ionisation (due to thin layers) is unlikely to occur in power devices as they have drift regions of several 10's of microns thick. Therefore, these two effects will not be covered in this section. Impact ionisation, also known as avalanche multiplication, occurs when the maximum electric field within the depletion region reaches a critical value, generally named critical electric field ( $\mathbb{E}_c$ ). When the critical electric field is reached, freed charge carriers will gain enough energy from the electric field to start an avalanche multiplication of electron-hole pairs within the depletion region through high velocity impacts with the lattice structure. This process increases the current through the depletion region to unsustainable level. For an abrupt junction, the breakdown voltage is related to the critical electric field and depletion width ( $W_{Dm}$ ) [61]:

$$V_{BD} = \frac{\mathbb{E}_c W_{Dm}}{2} = \frac{\varepsilon_s \mathbb{E}_c^2}{2qN_D} \quad (3.24)$$

This is illustrated in Fig. 3.16, where the breakdown voltage is the area under the electric field line when the peak electric field reaches the critical electric field value. The figure assumes the opposite side of the junction is metal or highly doped silicon, which means the depletion width on the opposite side will be negligible. The shape of the depletion layer will be different with graded junction or punch-through structures [61].

The second part of Eqn. 3.24 relates the breakdown voltage with the critical electric field

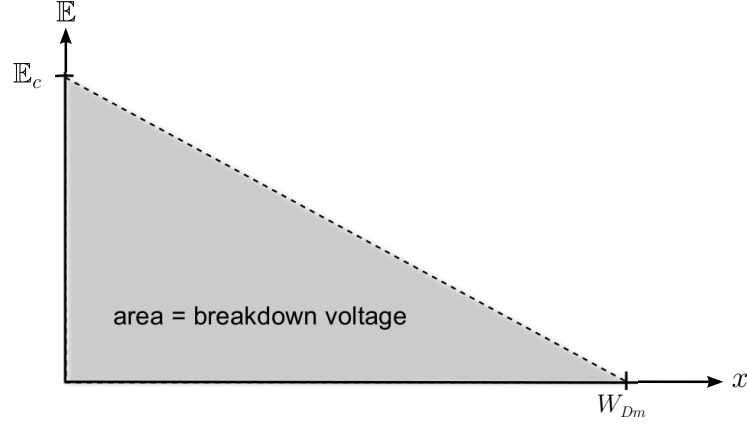


Figure 3.16: The relationship between electric field and depletion width, the area under the line indicates the breakdown voltage when the critical electric field has been reached for a punch-through device.

and the dopant concentration of silicon, where  $\varepsilon_s$  is the permittivity of silicon ( $\varepsilon_s = \varepsilon_{si}\varepsilon_0$ ). The equation indicates that higher breakdown voltages could be obtained with lower dopant concentrations. However, this relationship may not be valid at dopant concentrations higher than  $3 \times 10^{17} \text{ cm}^{-3}$  since other effects will contribute to the breakdown process [61]. The calculated relationship is shown in Fig. 3.17(a) [85]. The critical electric field is also lightly dependent on the dopant concentration, the dependence for abrupt PN junctions is presented in Fig. 3.17(b) and can be expressed as [61]:

$$\mathbb{E}_c = \frac{4 \times 10^5}{1 - (1/3) \log_{10}(N_D/10^{16})} \quad (3.25)$$

For abrupt junctions, the temperature dependence of the breakdown voltage was predicted by Crowell and Sze, the data is presented in Fig. 3.18 [86]. The figure presents the normalised breakdown voltages to 300 K for three different dopant concentrations, the breakdown voltages decrease when temperature is reduced and the rate of change with temperature is higher for lower doped silicon. Intuitively, the reason breakdown voltage decreases at lower temperatures is due to the increased electron-hole mobilities. Freed electrons and holes in the depletion region gain more energy from the same electric field. Therefore the impact ionisation process will be more efficient and the critical electric field will decrease.

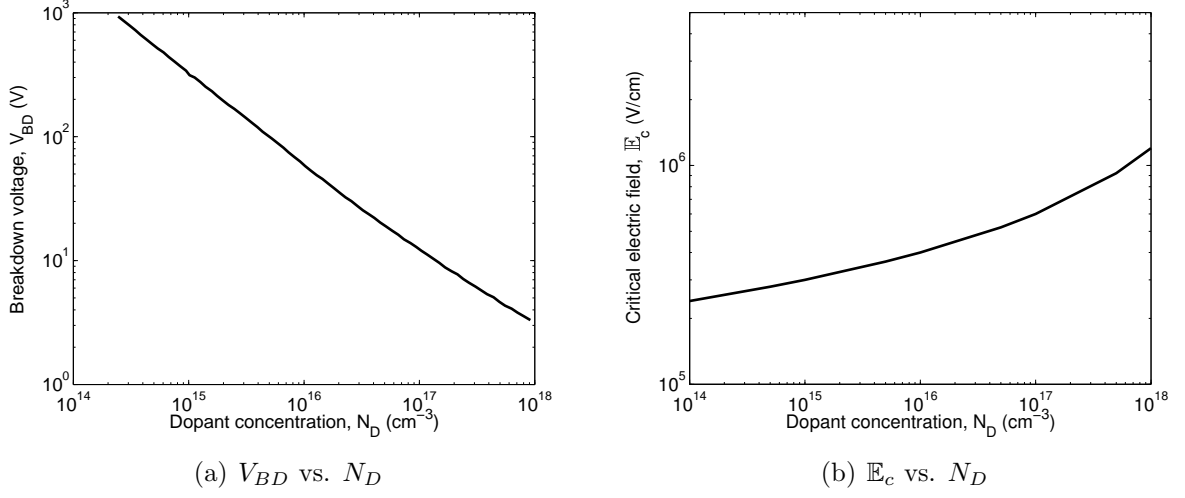


Figure 3.17: For abrupt PN junctions: (a) Breakdown voltage as a function of dopant concentration [85]. (b) Critical electric field as a function of dopant concentration [61].

#### 3.3.1 Silicon Limit Breakthrough with Super-Junction

For conventional unipolar devices, there is a fundamental limit to the lowest on-state resistance achievable at a given breakdown voltage. This can be seen from Eqn. 3.24, where there is a maximum dopant concentration and minimum drift region thickness that can be

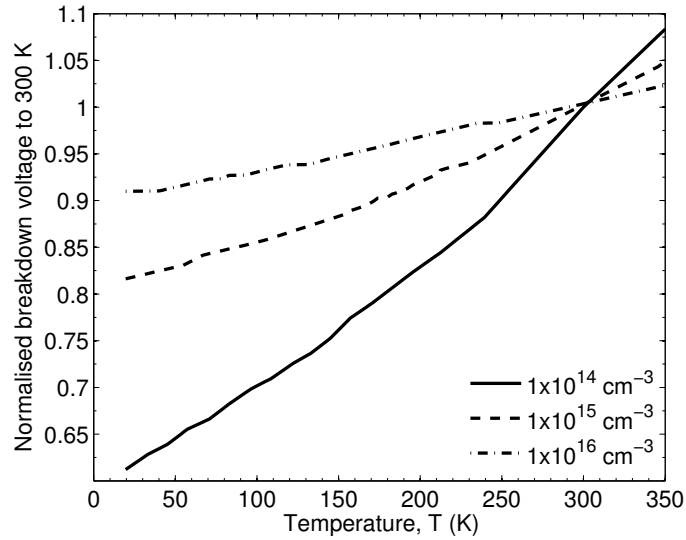


Figure 3.18: The predicted breakdown voltage of a silicon abrupt junction as a function of temperature for various dopant concentrations [86].

used for a certain breakdown voltage of a power device. For higher the breakdown voltages, the dopant concentration must be lower or the drift region must be thicker. This leads to a higher minimum on-state resistance. This is known as the fundamental silicon limit.

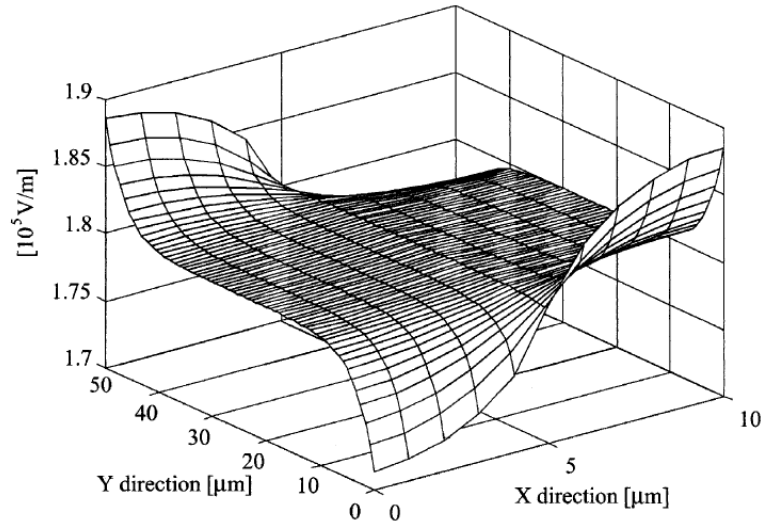


Figure 3.19: MEDICI simulated electric field profile of a SJ structure [87].

In recent years, a novel idea most commonly known as the super-junction (SJ) theory [31] [88] has managed to surpass the silicon limit. This is achieved by replacing the drift region of a device with alternating P and N pillars (See Fig. 2.16). This changes the electric field profile from an essentially one dimensional profile (for a conventional drift region) to a two dimensional profile. A MEDICI simulated example of the electric field profile is presented in Fig. 3.19 [87]. In this new structure, more electric field can be sustained under the curve across the Y direction, in comparison to the triangle shape electric field in Fig. 3.16. Due to the two dimensional shape of this electric field profile, higher dopant concentrations can be used as well as thinner drift regions. The breakdown voltage becomes essentially independent of the dopant concentration and only depends on the thickness of the drift region. At the same breakdown voltage, SJ devices can reduce the on-state resistance by a factor of five [32]. However, this requires the dopant concentration of the N and P pillars to be the same, charge imbalance between the alternating pillars can reduce the breakdown voltage substantially [89]. Furthermore, in order for the SJ effect to work, the pillar width



is also required to be small, especially at high dopant concentrations [34].

The physical breakdown process for a SJ structure is the same as conventional junctions. However, the dopant concentration would be higher. How the two dimensional electric field will affect the temperature dependence has not been found in any literature.

#### 3.3.2 Ionisation Rates

The impact ionisation process can be described by the ionisation rates of electrons and holes. If the impact ionisation is initiated by holes, the breakdown condition is given by the ionisation integral [61]:

$$\int_0^{W_{Dm}} \alpha_p \exp \left[ - \int_0^x (\alpha_p - \alpha_n) dx' \right] dx = 1, \quad (3.26)$$

If electrons initiate the breakdown condition, it is given by:

$$\int_0^{W_{Dm}} \alpha_n \exp \left[ - \int_x^{W_{Dm}} (\alpha_n - \alpha_p) dx' \right] dx = 1. \quad (3.27)$$

$\alpha_n$  and  $\alpha_p$  are electron and hole ionisation rates respectively. The temperature dependence of these two parameters are difficult to assess. In order to simplify the description of the breakdown process, the two ionisation rates can be combined to form a single effective ionisation rate ( $\alpha_{eff}$ ). Here, the breakdown condition is when the integration of the effective ionisation rate within the depletion width is equal to one:

$$\int_0^{W_{Dm}} \alpha_{eff}(\mathbb{E}) dx = 1. \quad (3.28)$$

The effective ionisation rate is dependent on the electric field and several models have been proposed to model this relationship [90] [85] [91]. They are all based on a simple formula expressed as.

$$\alpha_{eff} = a \exp(-b/\mathbb{E}), \quad (3.29)$$

where  $a$  and  $b$  are coefficients extracted from empirical measurements and are temperature dependent. Singh and Baliga [16] proposed a simpler temperature dependent empirical model based on Fulop's formula [92] where the effective ionisation rate is expressed as:

$$\alpha_{eff} = C\mathbb{E}^g, \quad (3.30)$$

and the breakdown voltage for an abrupt junction can be derived as:

$$V_{BD} = 0.5 \left( \frac{g+1}{C} \right)^{2/(g+1)} \left( \frac{qN_D}{\varepsilon_s} \right)^{(1-g)/(1+g)}, \quad (3.31)$$

$C$  and  $g$  have the following temperature dependence:

$$C = 2 \times 10^{-28} \exp \left( \frac{-16.22T}{300} \right), \quad (3.32)$$

$$g = 5.8 + 1.2 \left( \frac{T}{300} \right). \quad (3.33)$$

The simulated temperature dependence of  $\alpha_{eff}$  at different electric field strength and  $V_{BD}$  at different dopant concentrations are presented in Fig. 3.20. The model predicts a linear increase in ionisation rates and linear decrease in breakdown voltages with lower temperatures.

#### 3.3.3 Cosmic Radiation Effects

In addition to temperature, the breakdown behaviour of power devices is also subject to other external influences. One of the main effects is cosmic radiation or cosmic rays. Cosmic rays are highly energetic subatomic particles from outer space. The main source is the Sun but there are other galactic radiation sources such as supernova explosions. Cosmic rays consist of, but are not limited to, protons, alpha particles, neutrons, electrons, mesons and photons. Most cosmic rays never reach the earth's surface due to the funnelling effects of the Earth's magnetic field which focus the radiation towards the magnetic poles. However, neutrons are not affected by this geomagnetism since they have no electric charge. Therefore,

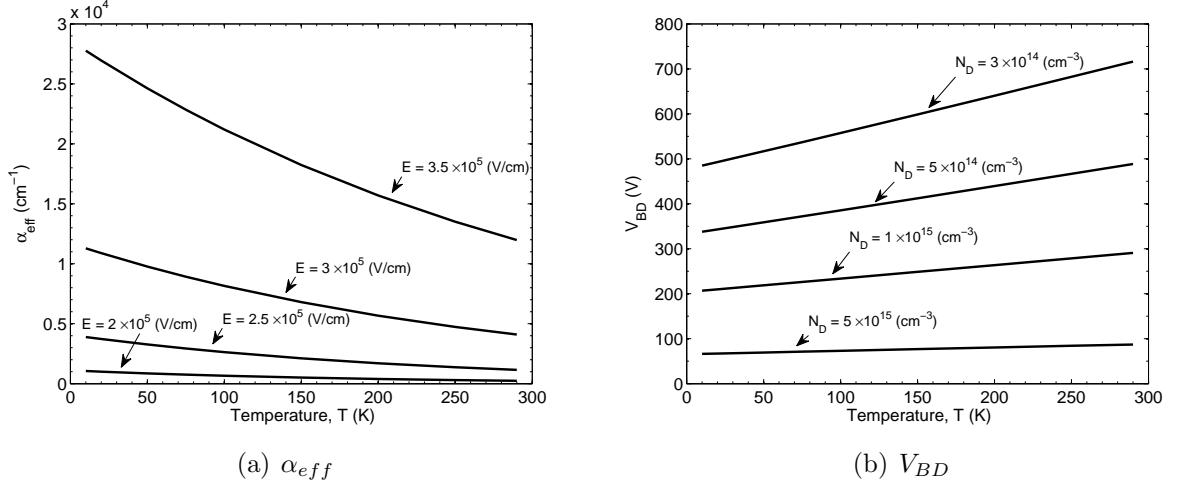


Figure 3.20: The simulated temperature dependence of (a)  $\alpha_{eff}$  at different electric field strength (Eqn. 3.30) and (b)  $V_{BD}$  at different dopant concentration (Eqn. 3.31).

they are known to be the main causes for device failures at sea level.

Device failures due to cosmic radiation in power devices have been known for a number of years [93]. Device failures under blocking conditions have been measured at different attitudes and conditions. Fig. 3.21 presents the number of device failures against time in the salt mine experiment by Kabza et al. The data clearly implies the relationship between device failures and the amount of cosmic radiation they receive. Only when the diodes used in the experiment 140 m below ground were the cosmic rays reduced enough to avoid any failures.

Cosmic ray induced failures are a particularly difficult effect to mitigate, since it is a failure effect without precursor and is purely a statistical process when shielding is not applied. In most cases, shielding is neither possible or appropriate which means power devices are not protected against this type of failure. Power devices are particularly affected by cosmic radiation due to their relatively large size and high voltage/power capability, which can result in device destruction. However, power devices can be design to reduce the effect of cosmic rays by improving their radiation hardness. Other methods include reducing the blocking voltage and decreasing the electric field across the device. Fig. 3.22 presents the predicted curves of temperature and altitude dependences of the failure rates for an

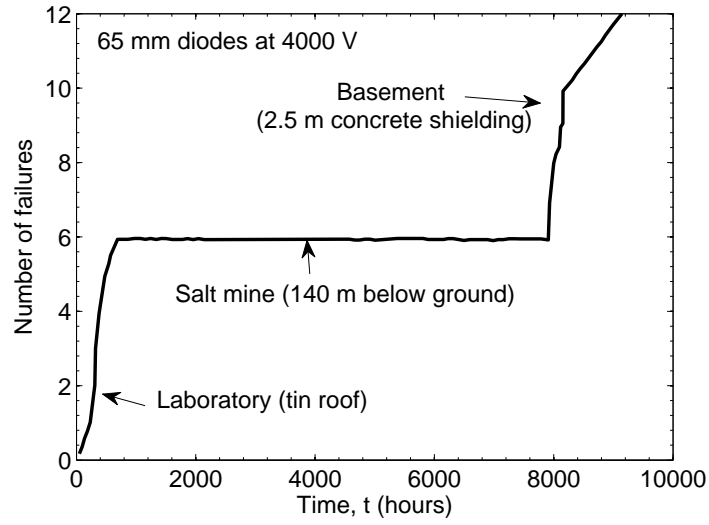


Figure 3.21: Device failure against time in the salt mine experiment [93].

IGBT based on empirical measurements by Kaminski [94]. The figures shows an increase in failure rates at lower temperatures and higher altitudes. These are particularly crucial for the intended application of this work where the power devices will be subject to cryogenic temperatures with relatively little shielding.

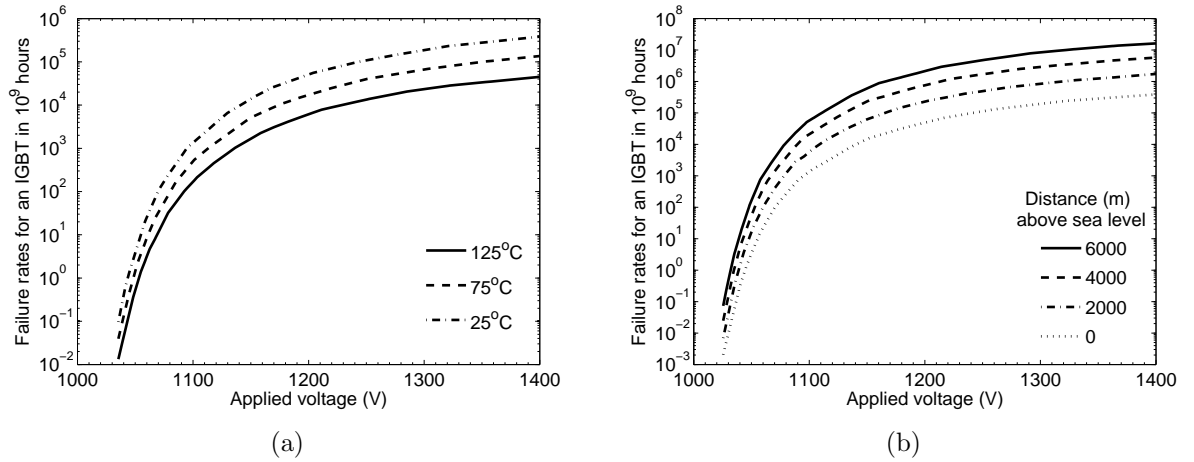


Figure 3.22: Failure rates against applied voltages for an IGBT at (a) different temperatures and (b) different altitudes [94].

### 3.4 Thermal Conductivity

The thermal conductivity of silicon is an important parameter for power devices because it describes the ability of the material to conduct away heat generated from the active region. Higher thermal conductivity would result in a device that is more thermally stable and reliable due to the lower  $\Delta T$  between the semiconductor and the packaging. The temperature dependent thermal conductivity of silicon has been measured in a number of studies. Its value at room temperature is generally accepted as  $1.3 \text{ W/cmK}$  [95] [96] [97]. This increases at lower temperatures as shown in Fig. 3.23. The figure shows the measured thermal conductivity of silicon ( $K$ ) down to 2 K. The temperature dependent thermal conductivity of intrinsic silicon exhibited non-monotonic behaviour. As the temperature is reduced from room temperature, the thermal conductivity of silicon rises to a peak at  $\sim 30 \text{ K}$  before rapidly reducing as  $T$  tends to 0 K. The figure also show the thermal conductivity for P-type silicon with a dopant concentration of  $1 \times 10^{15} \text{ cm}^{-3}$ . At temperatures above 100 K, its thermal conductivity is similar to intrinsic silicon and it is commonly assumed that the thermal conductivity of silicon is independent of dopant concentration at temperatures above 100 K. However, impurities inside the silicon will cause a reduction in the thermal conductivity at temperatures below 100 K.

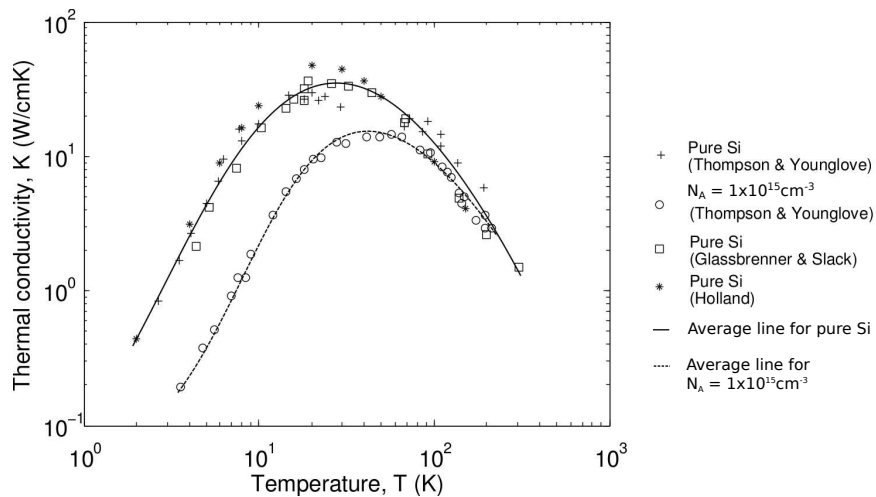


Figure 3.23: The measured thermal conductivity of silicon against temperature, + and o [95], □ [96] and \* [97].

## Cryogenic System and Device Characterisation Setup

The cryogenic behaviour of power devices is largely unknown below the liquid nitrogen temperature of 77 K. In order to investigate the feasibility of utilising power devices at cryogenic temperatures of 30 K, device characterisation from room temperature down to 20 K will be the core aspect of this work. This chapter describes the cryogenic system used in this study and the measurement setup.

### 4.1 Background

Initially, device characterisations were intended to be performed at the Converteam site in Rugby, UK. However, it was soon realised that the cryogenic system there was too big for this application. Therefore, a stand alone cryogenic system was needed which can reach temperatures as low as 30 K. By coincidence, the Nano-silicon group in the Physics department within the University of Warwick was at the time attempting to sell off a small cryogenic rig that was previously used to perform hall measurements down to 13 K, this is shown in Fig. 4.1. Therefore, it was decided to purchase this system and strip it down to the essential components and convert it to characterise power devices. This included adding an accurate temperature sensor and heater.

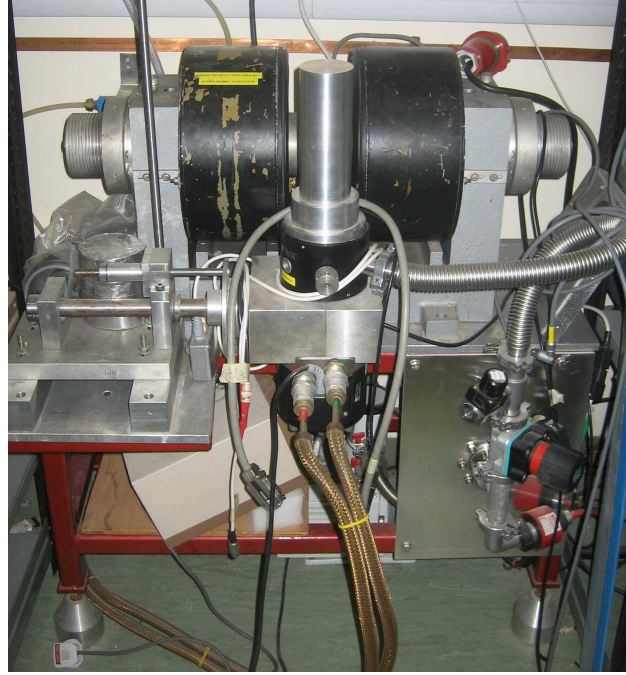


Figure 4.1: The initial cryogenic system designed to perform hall measurements.

## 4.2 Cryogenic System

Fig. 4.2 presents the cryogenic system configuration, it can be broken down into three main sub-systems:

- The cooling system and cryostat.
- The vacuum pump system.
- The temperature controller.

This section will briefly describe each sub-system. Further illustrations of the full cryogenic system can be found in Appendix D.

### 4.2.1 The Cooling System and Cryostat

The cryogenic cooling system is a closed cycle helium cryostat (Leybold RDK 10-320), with a modified aluminium outer and inner casing. The casings were modified for the previous hall measurement setup in order to fit between two magnets. The cooling system consists of

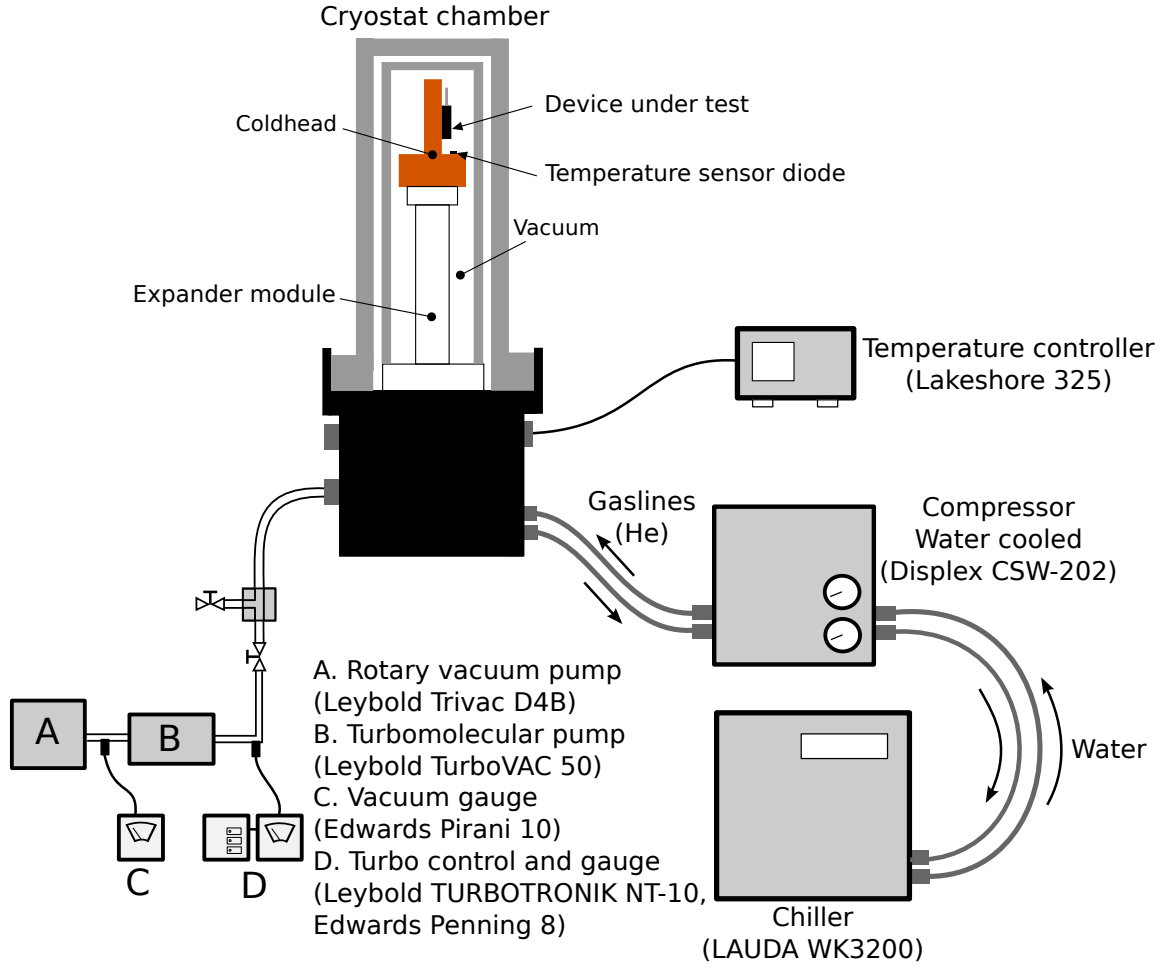


Figure 4.2: Cryogenic system configuration.

the expander module which expands helium vapour inside a chamber. The cooling process is based on the Joule-Thomson effect. The chilled module is thermally connected to the copper cold-head and therefore the temperature of the cold-head decreases. The compressor low pressure helium exhausts are returned to the compressor, cooled and pumped back to the expander module in order to continue the cycle. The high power water chiller circulates cooled water to keep the compressor at  $15^{\circ}C$ . Due to the relatively small cold-head of this cryogenic system, the size of the device footprint is limited to  $4\text{ cm} \times 2\text{ cm}$ , see appendix D for more details.



### 4.2.2 The Vacuum Pump System

Since the cold-head temperature will reach cryogenic temperatures, the internal environment of the cryostat has to be kept in high vacuum to stop ice formation on the cold-head and devices under test. The vacuum pump system consists of: a turbomolecular vacuum pump (Leybold TurboVAC 50), which can generate vacuum level down to  $10^{-8}$  mbar pressure; a Turbocontroller (Leybold Turbotronik NT-10) and gauges/heads (Edwards Penning 8/CP25-S); a rotary vane dual stage vacuum pump (Leybold TRIVAC D4B) for turbomolecular pump backing; vacuum gauges (Edwards Pirani 10) and head (Edwards PR10-K) and a mechanical gas valve.

### 4.2.3 The Temperature Controller

The temperature of the cold-head has to be monitored and controlled in order to estimate the temperature of the power device attached. Since the cooling system simply chills the cold-head to 13 K, obtaining a stable temperature above 13 K is performed by heating the cold-head while balancing the cooling action of the cooling system. The cold-head is heated by a resistive ( $27\ \Omega$ ) heater attached to its base. The temperature sensor diode (Lakeshore DT-670) also attached to the cold-head (close to the device under test) measures the exact temperature of the cold-head. The actual control is by the temperature controller (Lakeshore 325) which utilises proportional-integral-derivative (PID) control algorithms to control the heater to match the measured temperature with the desired temperature value. The temperature sensor diode wiring is thermally sunked to the cold-head by wrapping it around the side of cold-head, this is done to minimise external heat leakage which could affect the temperature measurement of the sensor diode.

## 4.3 On-state and Breakdown Measurement System

Fig. 4.3 presents the on-state and breakdown measurement system. The cold-head inside the cryostat chamber has a vertically orientated detachable copper plate, which enables through hole power devices to be mechanically and thermally attached to the cold-head to ensure

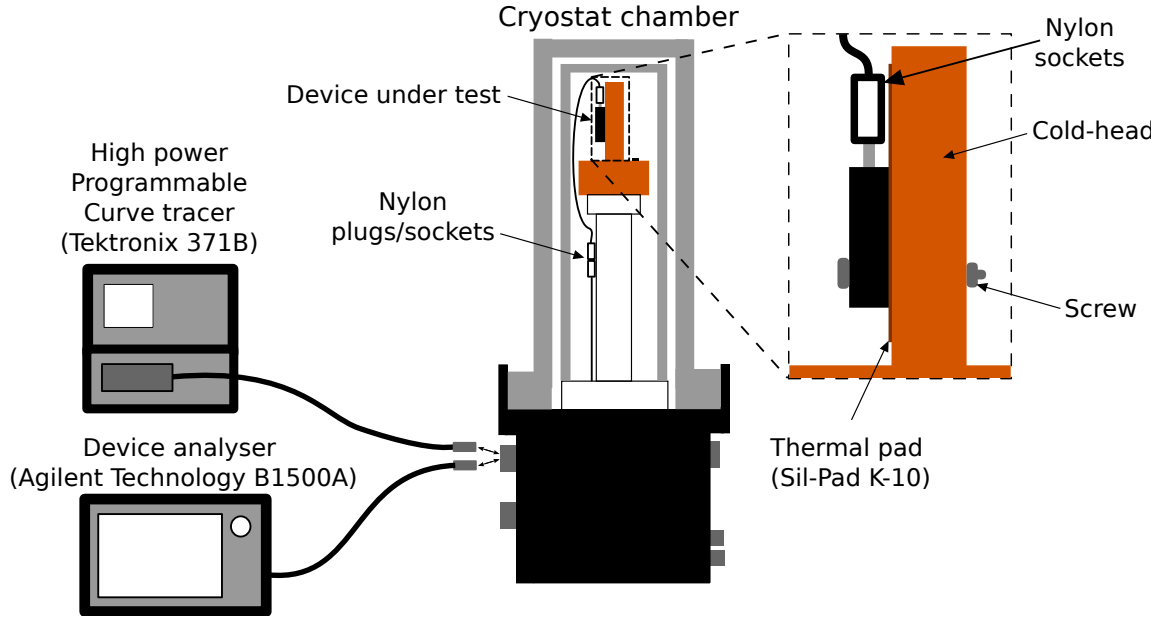


Figure 4.3: On-state and breakdown measurement system configuration.

minimum temperature difference between the cold head and the measured device. Also, since some power devices have an active terminal as the back plate, a thin layer of silicone insulating thermal pad (Sil-Pad K-10) was used to electrically isolate the device from the copper cold-head while maintaining a good thermal contact. Nylon sockets were also used for the electrical connections to make power devices easily interchangeable between measurements. All on-state characterisation was measured with the kelvin connection method, also known as four-point probes method, which uses separate pairs of current carrying and voltage sensing electrodes to make more accurate measurements than traditional two terminals measurements. The on-state behaviour and breakdown voltage measurements were performed by a high power programmable curve tracer (Tektronix® 371B), which is a power device characterisation machine normally used to verify device performance and failure analysis. Both on-state behaviour and breakdown measurements were performed without physically changing the electrical connections by using a modified switch box connection (see appendix D). The curve tracer has a high DC resolution down to 1 pA or 2  $\mu$ V. Low current measurements for the Schottky diodes were performed by a semiconductor device analyser (Agilent Technology B1500A). Modified adapters have been used in both machines in order to connect

to the cryostat rig.

## 4.4 Switching Measurement

For the power MOSFET switching measurements, a chopper cell test circuit was set up to carry out the double pulse switching test. The circuit is shown in Fig. 4.4. The double pulse consists of two successive pulses with a short period in between. The first is a long pulse designed to energise the inductor, then a short off pulse to ensure the power MOSFET is switched off. There is then, a short on pulse to measure the turn on and turn off behaviour of the power MOSFET. A Schottky diode and MOSFET were placed in the cryostat chamber to be cooled and the remainder of the circuit was kept at room temperature. The gate of the power MOSFET was controlled by sending a double pulse signal at 15 V to the gate terminal. The power supply was at 20 V, the DC (direct current) link capacitor has a value of 200  $\mu\text{F}$  and the inductor has a value of 500  $\mu\text{H}$ . The measurements were recorded by a four channel oscilloscope (Tektronix TDS5054B), the double pulse was generated by a function generator (Tektronix AFG3022) and the gate driver is a purpose build circuit.

Unfortunately, the cryostat chamber has long DC bus wiring to connect the high vacuum adapters near the base of the cryostat to the cold-head. This results in a large stray inductance. Bus bar connections with low stray inductance [42] were not possible due to the space restriction within the cryostat. To reduce the stray inductance, twisted wires were used within the cryostat and the wiring outside was kept to an absolute minimum. Fig. 4.5 illustrates the long wiring inside the cryostat. The stray inductance was calculated to be  $\sim 680$  nH. A high stray inductance can cause large voltage overshoot during switching measurements. In order to reduce this effect, a 50  $\Omega$  gate resistor was used to reduce the rate of change in the gate voltage.

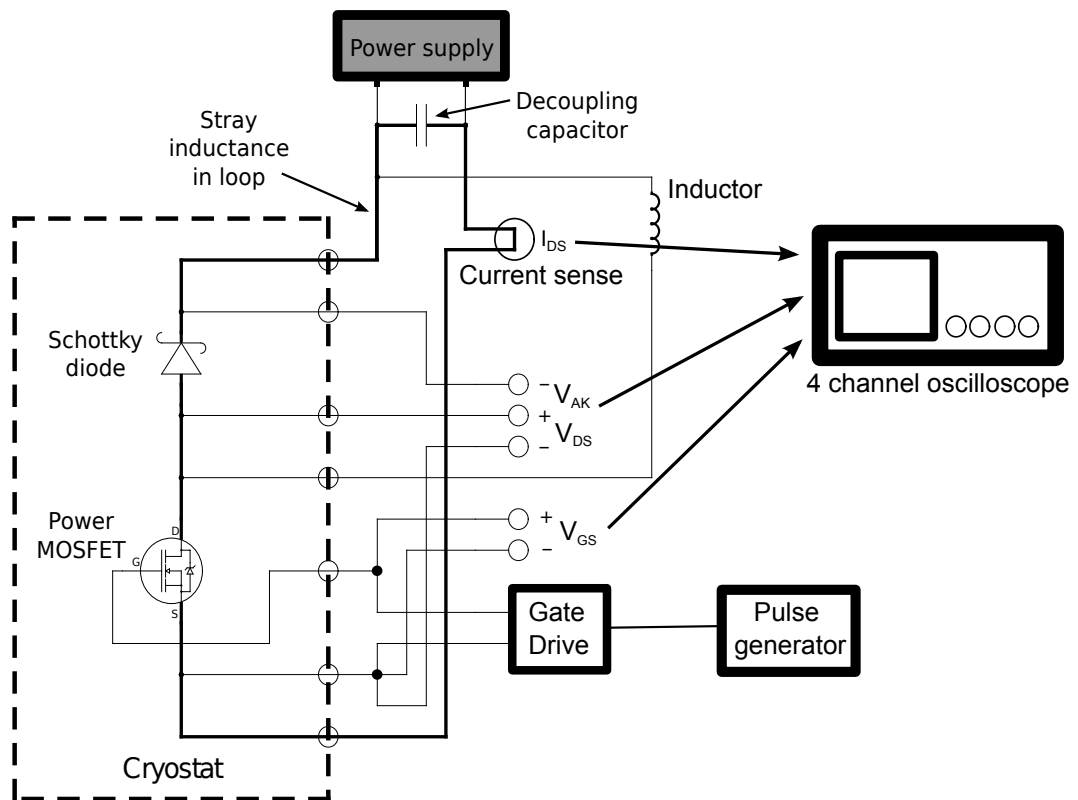


Figure 4.4: The chopper cell circuit for the switching measurements.

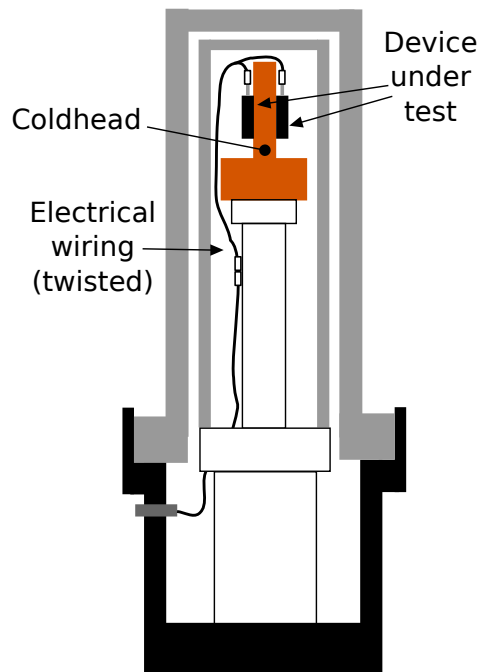


Figure 4.5: Illustration of the long DC bus wiring inside the cryostat chamber.

# Cryogenic Characterisations of Power MOSFETs, HEMTs and Schottky Diodes

From analysing the known behaviour of power devices in chapter 2, the main conclusion is that the focus of this work would be on power MOSFETs as these devices should be able to achieve the lowest on-state resistance. This chapter will present the measured cryogenic behaviour of several types of power MOSFET down to 20 K. These include the HEXFET®, the high voltage PowerMESH™, super-junction (SJ) MOSFETs such as CoolMOS™ and MDMesh™, as well as SiC power MOSFETs. The rest of the chapter will present the measured cryogenic behaviour of GaN HEMTs and power Schottky diodes, including: conventional silicon power Schottky diodes, TMBS diodes, gallium arsenide Schottky diodes and silicon carbide Schottky diodes.

## 5.1 Power MOSFETs

In the introduction to power MOSFETs in chapter 2.1, it is clear that their known behaviour at cryogenic temperatures does not extend below 77 K (with the exception from Karunanithi et al. [26], which measured down to 4 K). Therefore, a more comprehensive investigation was required to analyse the power MOSFET behaviour at lower temperatures and over a wider range of voltage and current ratings.

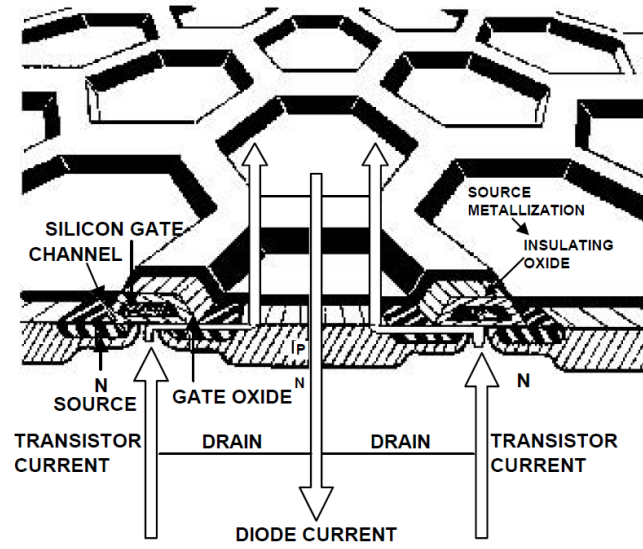


Figure 5.1: Illustration of the HEXFET® cell structure [98].

### 5.1.1 HEXFET®

The HEXFET® is a well known class of power MOSFET from International Rectifiers Inc. (IR). It utilises a hexagonal cellular structure in the horizontal plane to optimise the current handling capability of the device. The hexagonal cellular structure is illustrated in Fig. 5.1 [98]. The device structure in the vertical plane is the vertical diffused MOS (VDMOS) structure, identical to the basic vertical power MOSFET structure presented in Fig. 2.13. This simple, conventional structure makes the HEXFET an ideal device to use as a benchmark against which more complicated structures can be compared.

#### 5.1.1.1 200 V HEXFET

A 200 V HEXFET (IRFP4668PbF, rated at 130 A, TO-247AC package) was measured from a temperature of 20 K, with increments of 10 K per step, up to 100 K. The room temperature behaviour is also presented for reference. This device has a typical drain source resistance of 8 mΩ at 300 K. The forward and reverse IV characteristics of this HEXFET at different gate voltages are presented in Fig. 5.2. The change in gate threshold voltage with temperature was also measured and is presented in Fig. 5.3(a). The data showed that the gate threshold

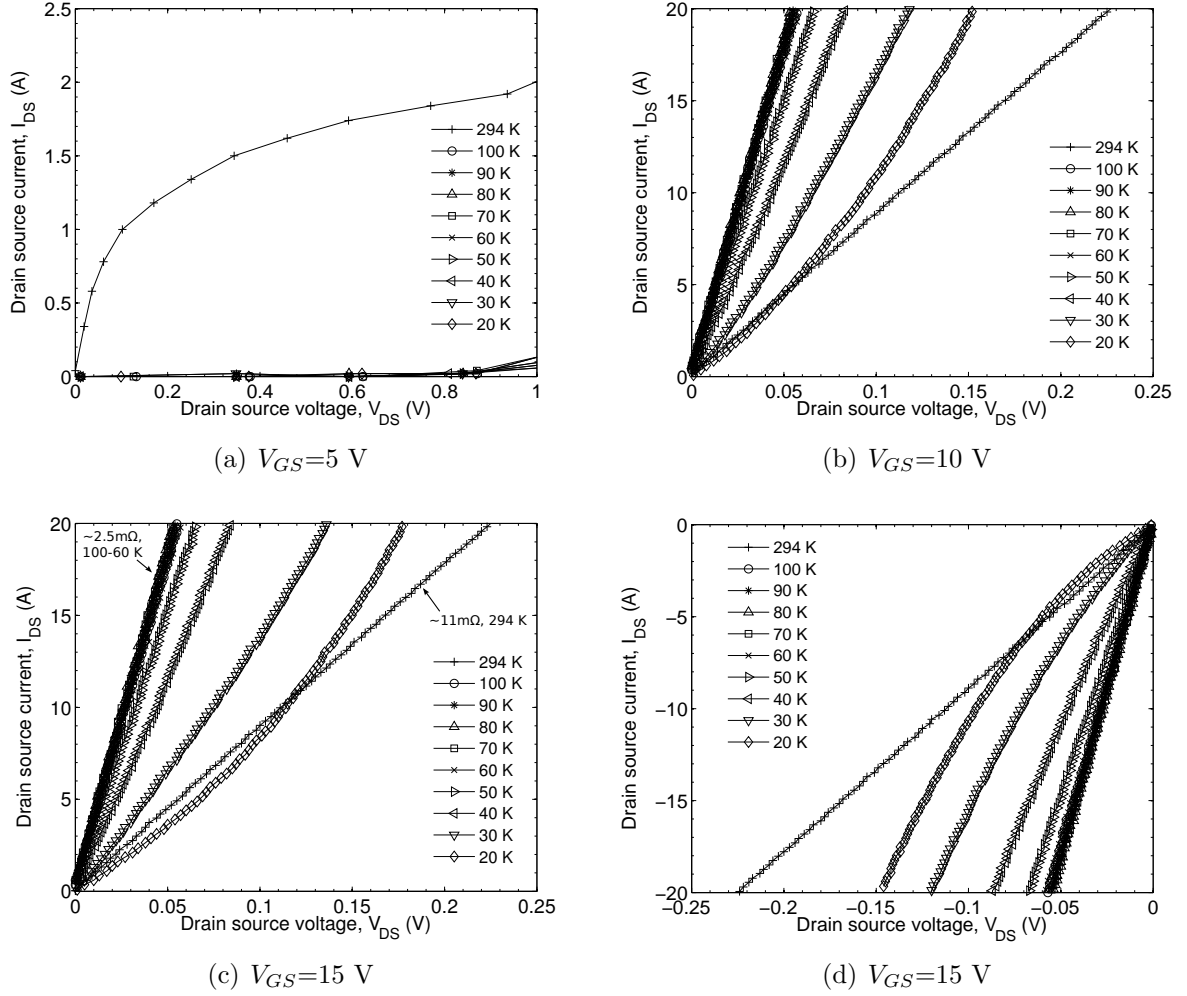


Figure 5.2: The temperature dependent forward IV characteristics of a 200 V HEXFET at (a)  $V_{GS} = 5$  V, (b)  $V_{GS} = 10$  V, (c)  $V_{GS} = 15$  V and the reverse IV characteristics at (d)  $V_{GS} = 15$  V.

voltage was 1.21 V higher at 20 K than at room temperature. At 100 K,  $V_{Gth} \simeq 5.65$  V, this means that at temperatures below 100 K, when  $V_{GS} = 5$  V the device will not turn on, as shown in Fig. 5.2(a). The IV characteristics are fairly similar for  $10 \text{ V} < V_{GS} < 15 \text{ V}$  with the exception of the measurements taken at 30 K and 20 K. The reverse IV characteristics show symmetrical behaviour in the third IV quadrant. It is clear from the data that temperature points from 100 K to 60 K are very closely matched and only begin to degrade below 50 K. However, the IV characteristics above 30 K are still better than room temperature.

The measured IV characteristics of the reverse body diode are presented in Fig. 5.3(b) for



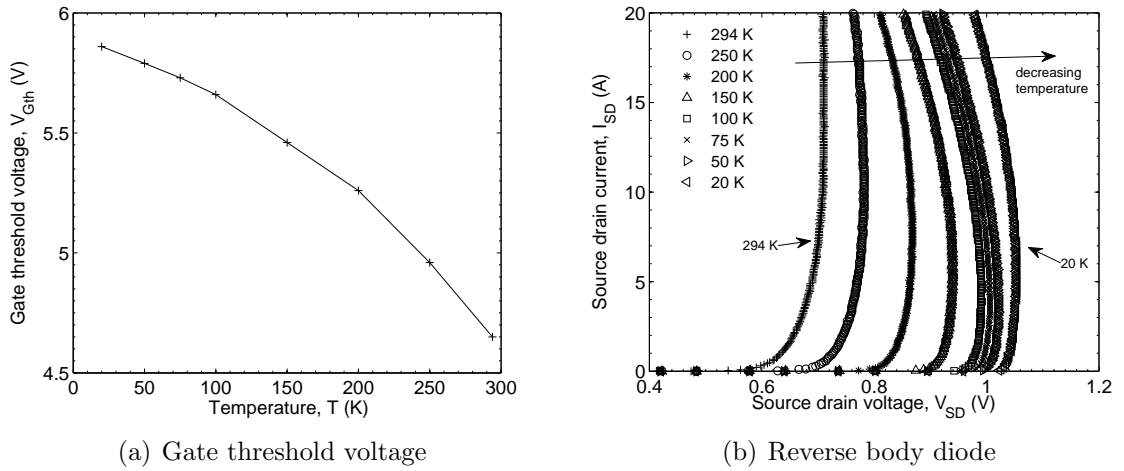


Figure 5.3: The temperature dependent (a) gate threshold voltage  $V_{Gth}$  and (b) IV characteristics of the reverse body diode of the 200 V HEXFET.

temperatures of 294 K, 250 K, 200 K, 150 K, 100 K, 75 K, 50 K and 20 K. The turn-on voltage of the body diode increased at lower temperatures. It increases steadily as temperature reduces from 300 K down to 100 K and saturates at  $\sim 1.05$  V at temperatures below that. One interesting behaviour is that the body diode experiences lower resistance at higher current levels and this becomes more pronounced at lower temperatures. However, this behaviour was observed only in the 200 V HEXFET device and the exact reason is unknown.

For conventional operating temperatures, a small variation in device performance is generally expected between devices of the same part number. However, since HEXFETs were not designed with the intention of operating at cryogenic temperatures, variations between devices in these conditions are unknown. In order to identify these variations, five 200 V HEXFETs were measured and compared. Within these devices, A1 through to A4 were from the same manufactured batch, whereas device B1 was from a different batch. The measured on-state resistances, ( $R_{ON}$ ) of the five HEXFETs are presented in Fig. 5.4.  $R_{ON}$  is defined as the inverse of the gradient of the linear region of the on-state curve of the MOSFET (from  $I_{DS} = 0$  to the start of the knee curve, see inset of figure).  $R_{ON}$  is 3.6 times lower at 80 K than at room temperature. This is comparable to the factor of four figure presented by Mueller at 77 K [99]. The results clearly show an optimum temperature range between

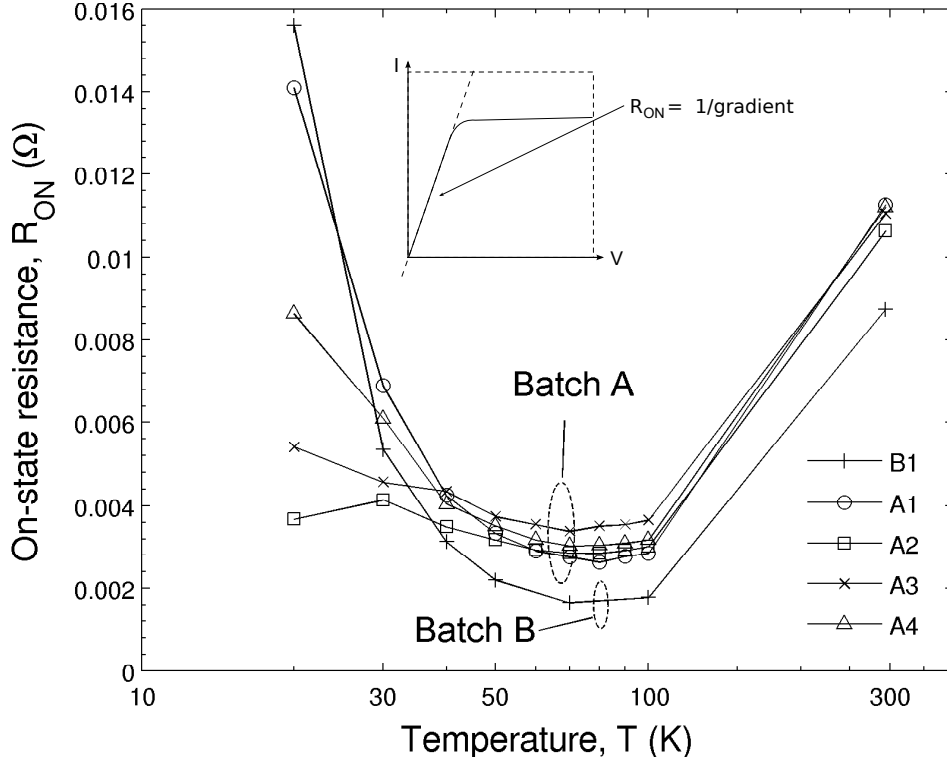


Figure 5.4: The measured temperature dependent on-state resistance,  $R_{ON}$  of the five 200 V HEXFETs.

60 K and 90 K, where  $R_{ON}$  is the lowest. For the four devices from batch A, there are small differences in the  $R_{ON}$  above 50 K, at an average variation of 0.7 mΩ. This is expected from the minute differences between the dopant profiles of each device. However, below 40 K, the measurements exhibited major variations between the four devices. At 20 K, A1 has the highest  $R_{ON}$  of 14.1 mΩ; whereas A2 has the lowest  $R_{ON}$  of 3.7 mΩ, a range of 10.4 mΩ. The device from batch B has a lower  $R_{ON}$  in the optimum temperature range compared to the devices in batch A. At 70 K, it is 1.4 mΩ lower than the average  $R_{ON}$  from batch A. However, it has a higher  $R_{ON}$  at 20 K than any devices in batch A.

At temperatures below 40 K, three out of the five HEXFETs exhibited voltage dependent on-state resistance in the ohmic region of their IV characteristics. This is especially evident in devices A1 and B1. The on-state resistance, shown in Fig. 5.4, does not account for this voltage dependence as it presumed the profile was linear in the linear region. The IV

measurements are presented in Fig. 5.5. At 30 K, both devices deviated from the linear ohmic behaviour as the drain-source voltage increased. This behaviour becomes more pronounced at 20 K. The same effect was observed in device A4 but was less pronounced. For the remaining two MOSFETs, device A2 and A3, no voltage dependent behaviour was observed at the current level measured.

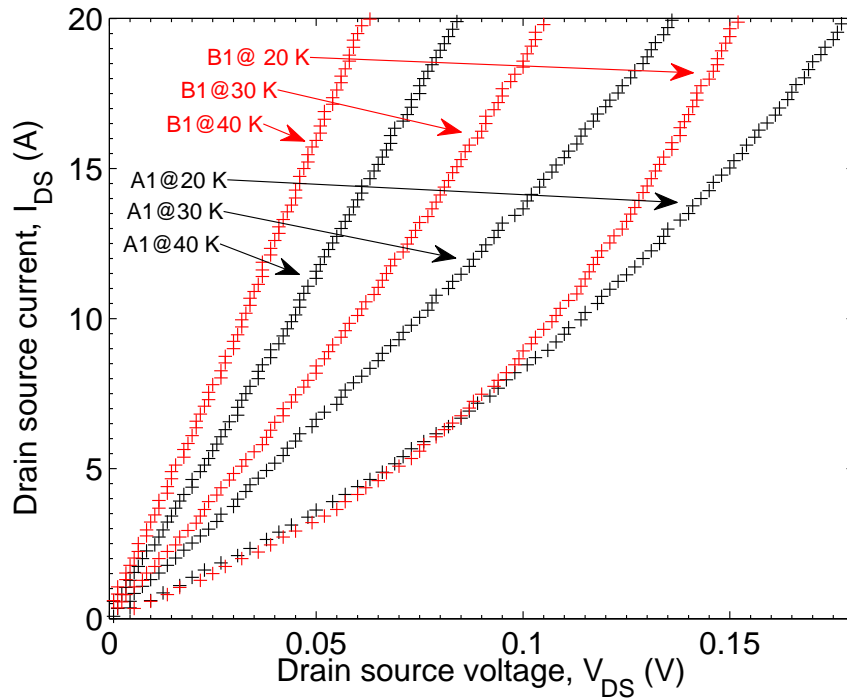


Figure 5.5: The non-ohmic behaviour at temperatures below 40 K for A1 and B1.

The instantaneous power loss from 20 K to 110 K was measured at 18 A and is presented in Fig. 5.6. It was measured at one minute intervals for 20 minutes. The supplied voltage was pulsed at 300 *ms* intervals with the gate voltage held at 15 V. The average change in power loss per second with temperature is also presented in the figure. Below 80 K, due to the negative temperature coefficient of the on-state resistance, the average power loss decreases over time due to self heating. However, it is important to note that for the devices that exhibited voltage dependent on-state resistance at temperatures below 40 K would have higher  $R_{ON}$  at lower current levels. In this case,  $R_{ON}$  is no longer constant and the power loss dependence on voltage is no longer linear. Above 80 K, the behaviour returns to a positive

temperature dependence and the power loss increases over time as the junction temperature rises.

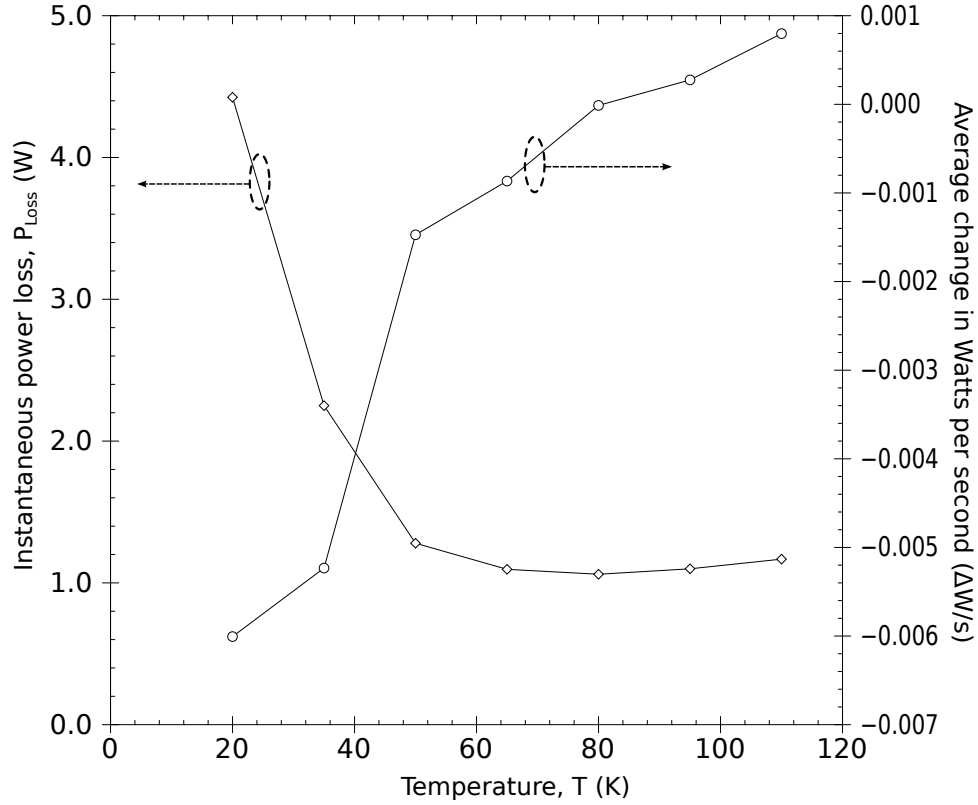


Figure 5.6: ◇ - Measured temperature dependent instantaneous power loss and ○ - the average change in power loss per second between 20 K and 110 K.

The measured breakdown voltages of the five HEXFETs from 20 K to 100 K are presented in Fig. 5.7, the breakdown voltages at room temperature are also added as reference. The data shows that breakdown voltage decreases as temperature decreases. The behaviour is identical between all the measured devices with  $V_{BD}$  an average of 24% lower at 20 K than at room temperature. All devices from batch A have near identical results, however the device from batch B behaves in the same manner but has a breakdown voltage that is consistently lower than batch A. This indicates that the device from batch B may have a thinner or more highly doped drift region when compared to batch A. This correlates with the lower on-state resistance shown in Fig. 5.4.

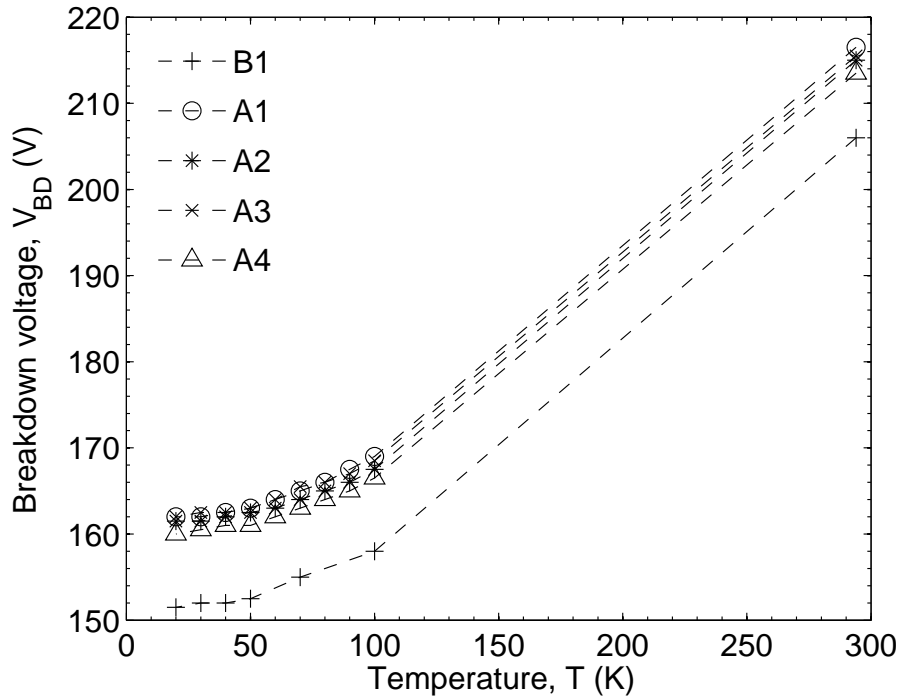
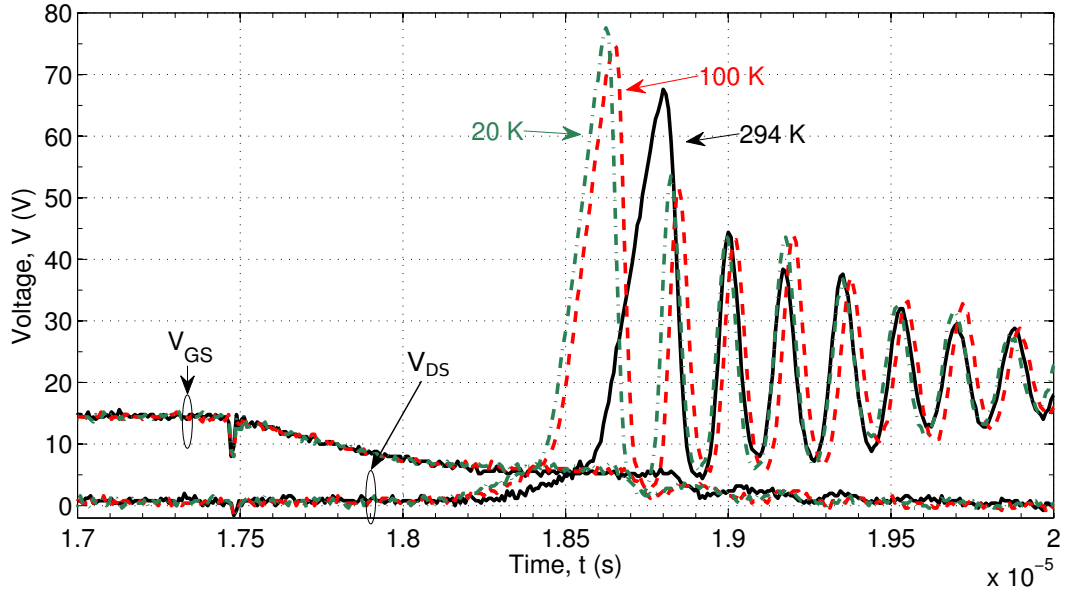


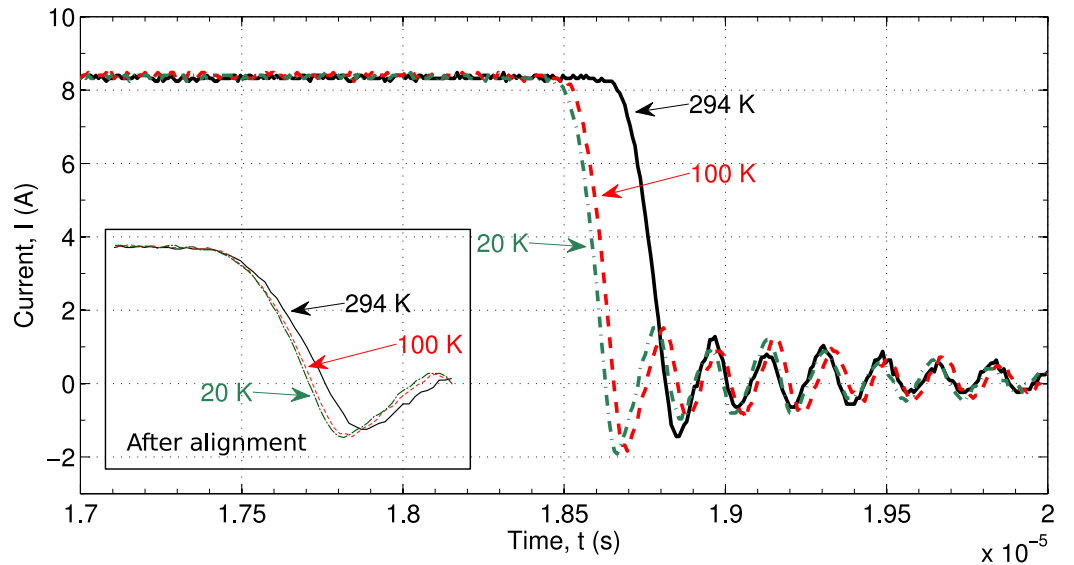
Figure 5.7: Measured temperature dependent breakdown voltages for the five power HEXFETs.

#### 5.1.1.2 Switching behaviour 200 V HEXFET

Using the switching measurement setup discussed in Chapter 4.4, the switching behaviour of a 200 V HEXFET was measured at 294 K, 100 K and 20 K. Fig. 5.8(a) presents the drain-source voltage waveforms at turn off and Fig. 5.8(b) presents the drain-source current waveforms at turn off. The measured gate voltage waveforms are also presented for reference. The two cryogenic measurements exhibited increased voltage overshoot when compared with the room temperature measurement. This correlates with the higher negative  $di/dt$ , as shown by the aligned data in the inset of Fig. 5.8(b). The magnitude of the overshoot is directly related to the parasitic stray inductance within the circuit, and the drain-source voltage oscillation is caused by the drain source capacitance, the stray inductance and the drain-source resistance forming a LCR resonant oscillator. At cryogenic temperatures, the combined effects of increased voltage overshoot and decreased breakdown voltage will be a critical factor in circuit design. This also emphasises the importance of minimising the



(a) Turn-off voltage



(b) Turn-off current

Figure 5.8: The temperature dependent (a) turn-off voltages and gate voltages and (b) turn-off currents at 294 K, 100 K and 20 K of a 200 V HEXFET.

stray inductance in the DC bus wiring in any circuit configuration operating at cryogenic temperatures. The power loss due to switching is dominated by the turn off loss. However due to the reduction in the turn off period, the overall energy loss reduces at cryogenic

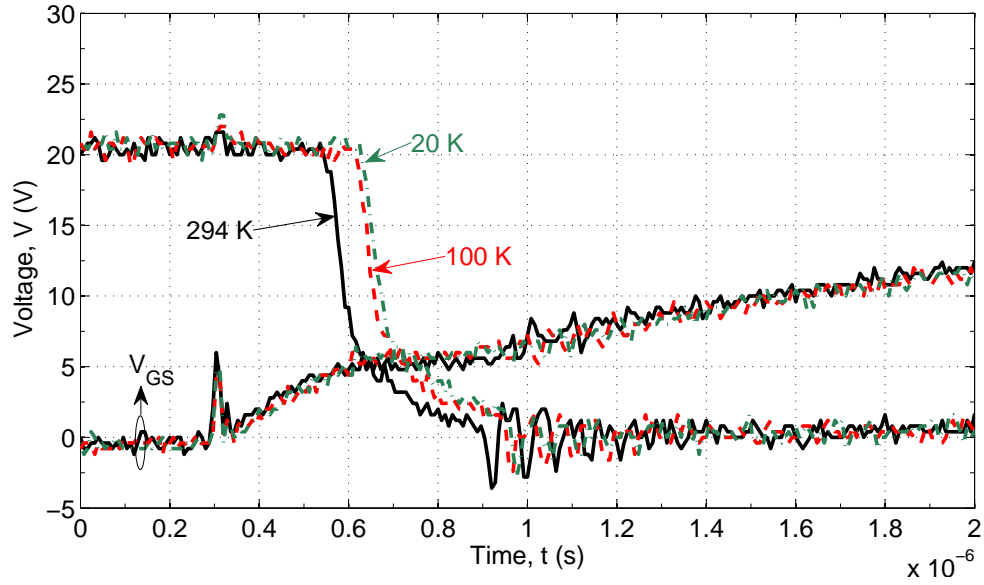
temperatures

Turn on waveforms from the same test are presented in Fig. 5.9; the gate voltage waveforms are also added for reference. For the turn on voltage waveforms, there is relatively little voltage undershoot and the current waveform exhibited minimal current oscillations. This means that the turn on event of the power MOSFET is quite stable and not critical in terms of voltage undershoot. The diode waveforms also exhibited virtually zero reverse recovery which is expected from a Schottky diode.

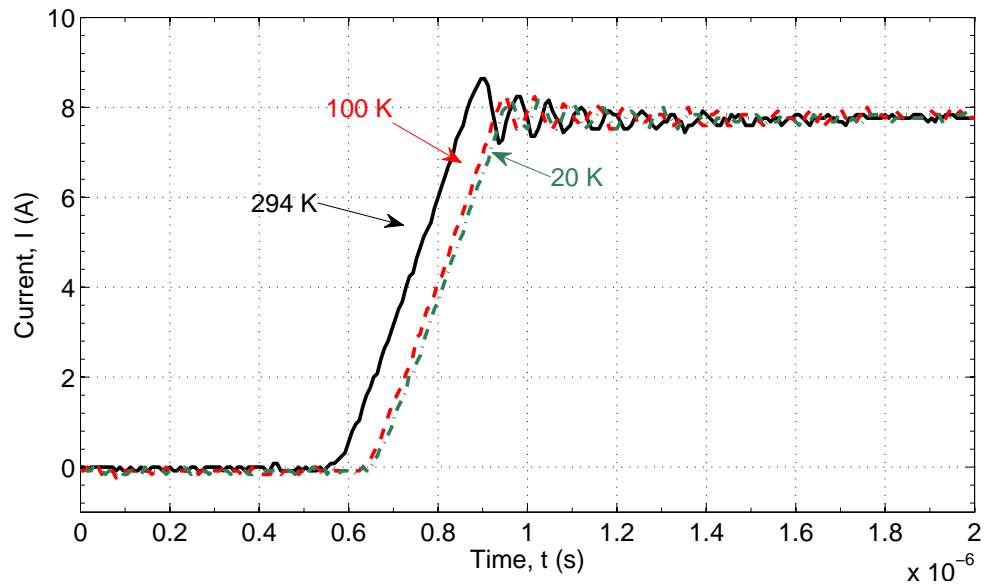
Another notable difference between the switching waveforms at room temperature and cryogenic temperatures is the timing between the changing states. During turn off events, the drain source voltage and current begin to turn off just over  $\sim 2 \mu\text{s}$  earlier at 100 K compared to room temperature, as shown in Fig. 5.8(a) and 5.8(b). The timing differences are primarily driven by the temperature dependent gate threshold voltage of the HEXFET. The threshold voltage was measured and it is  $\sim 1.2 \text{ V}$  higher at 20 K than at room temperature. This means it will take longer to reach the required gate voltage to turn on the device (hence the delay during turn on events) and a shorter time to reduce the gate voltage during turn off. The overall effect is that the voltage off period across the power MOSFET will become slightly narrower; whereas, a voltage on period will become slightly wider. These can have undesirable effects in switch mode power applications, especially in high frequency switching applications. However, since the measurements were performed with a high gate resistance to reduce the parasitic effects caused by the high stray inductance of the cryogenic rig, the timing differences would be magnified.

#### 5.1.1.3 P-channel HEXFET

Karunanithi et al.'s measurements of the p-channel MOSFET, shown in Fig. 2.14(c), suggests that the p-channel MOSFET may experience carrier freeze-out effects at a lower temperatures than the n-channel MOSFET. However, data from the last section shows that the 200 V rated n-channel HEXFET doesn't experience any degradation in performance until 50 K and only some suffer serious degradation below 40 K. Here, a -150 V p-channel HEXFET (IRF6215PbF, 13 A, in TO-220AB package) was characterised at the temperatures



(a) Turn-on voltage



(b) Turn-on current

Figure 5.9: The temperature dependent (a) turn-on voltages and gate voltages and (b) turn-on currents at 294 K, 100 K and 20 K of a 200 V HEXFET.

of 294 K, 250 K, 200 K, 150 K, 100 K, 75 K, 50 K and 20 K. The forward IV characteristics at different gate voltages and on-state resistance at  $V_{GS} = -15$  V are presented in Fig. 5.10. The data at temperatures of 20 K, 50 K and 75 K are highlighted with red, blue and purple



respectively to differentiate them from the higher temperature measurements.

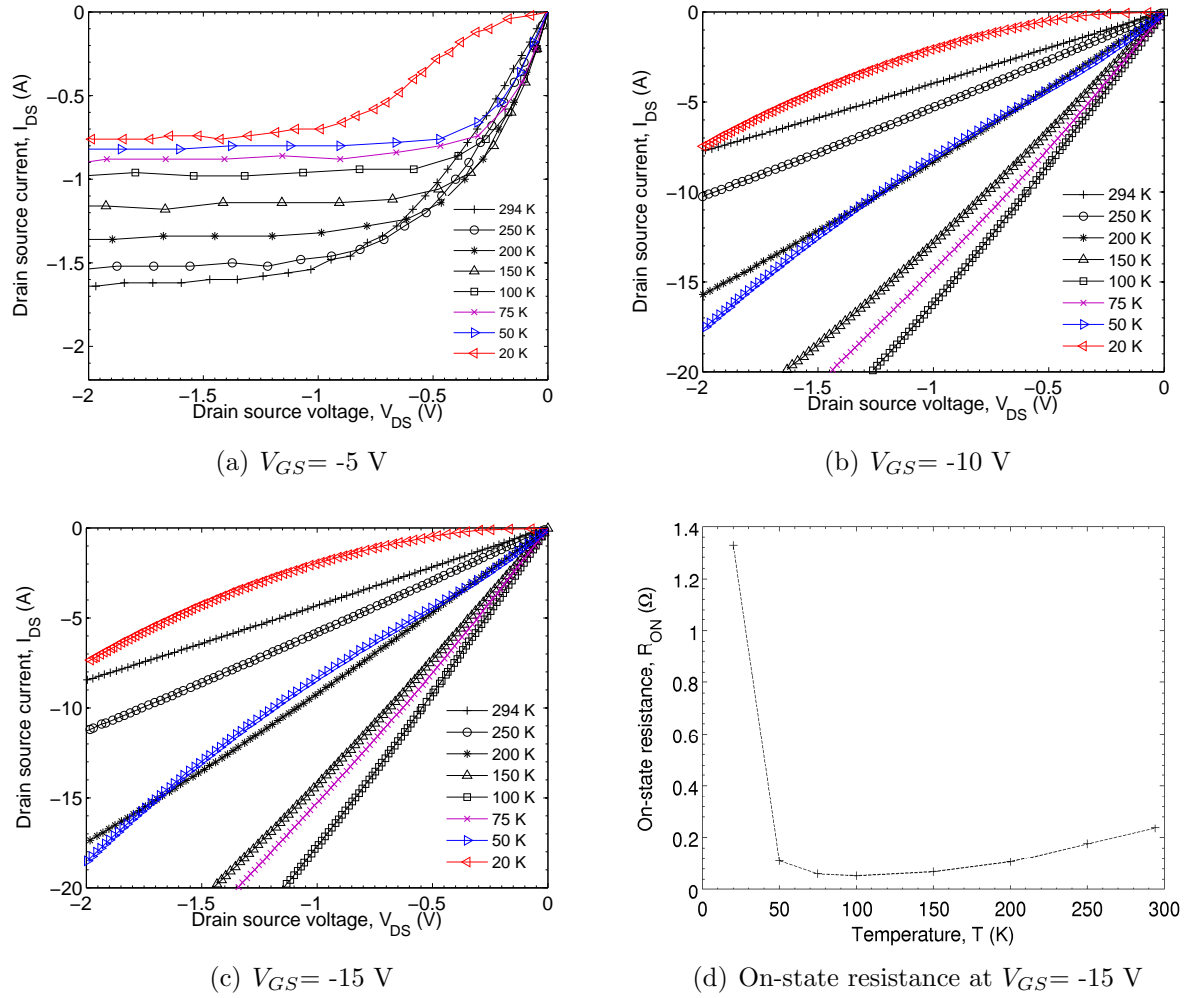


Figure 5.10: The temperature dependent IV characteristics of a -150 V p-channel HEXFET at (a)  $V_{GS} = -5$ , (b)  $V_{GS} = -10$ , (c)  $V_{GS} = -15$  V and (d) the on-state resistance at  $V_{GS} = -15$  V.

At  $V_{GS} = -5$  V, the HEXFET was only weakly turned on. The device exhibits low current gain with steadily decreasing saturation currents at lower temperatures. At 20 K, the linear region of the IV characteristics shows non-ohmic behaviour with the on-state resistance reducing with higher voltage until the saturation current is reached. The IV characteristics between  $V_{GS} = -10$  and  $-15$  V were very similar. Degradation was observed at temperatures as high as 75 K, with notable non-ohmic behaviour as high as 50 K. The on-state resistance was

4.3 times higher at room temperature than at 100 K but was 5.6 times higher at 20 K than 100 K. However this does not account for the lower on-state resistance at higher drain-source voltages.

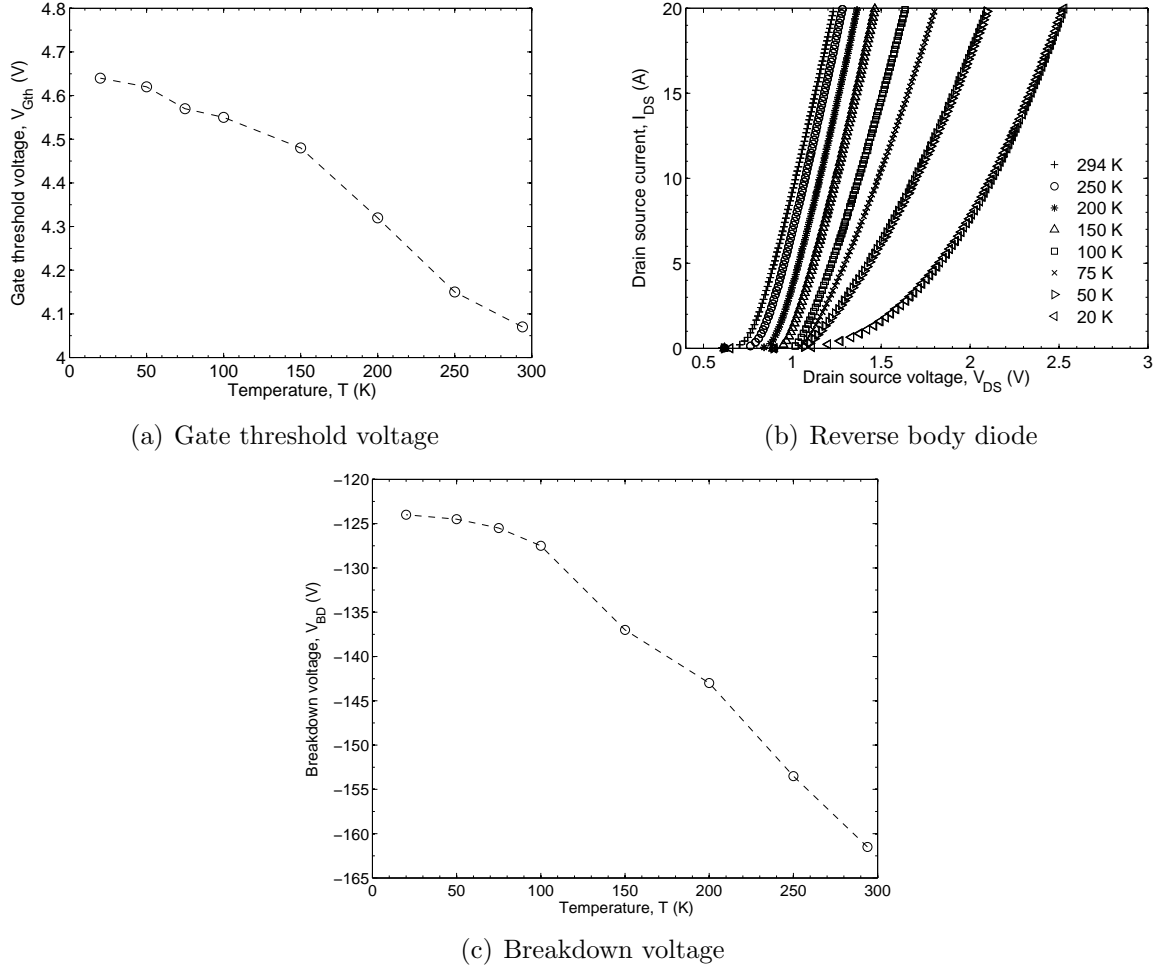


Figure 5.11: The measured (a) gate threshold  $V_{Gth}$ , (b) IV characteristics of the body diode and (c) breakdown voltages of a -150 V the p-channel HEXFET with temperature.

The temperature dependent gate threshold of the p-channel HEXFET is presented in Fig. 5.11(a). The data shows that the threshold voltage increases at lower temperatures. However, the increase as temperature is reduced to 20 K is only  $\sim 0.5$  V, much smaller variation than the n-channel HEXFET in Fig. 5.3(a). The IV characteristics of the reverse body diode are presented in Fig. 5.11(b). Unlike the body diode of the n-channel HEXFET, the p-channel HEXFET body diode exhibited no negative change in resistance

at any temperatures but did exhibit slow turn-on at 20 K.

The breakdown voltage of the p-channel HEXFET is presented in Fig. 5.11(c). It shows an approximately linear decrease as temperatures is reduced from room temperature to 100 K and saturates at temperatures below 100 K. The breakdown voltage was  $\sim 23\%$  lower at 20 K compared to room temperature, which is comparable to the  $\sim 24\%$  decrease for the n-channel HEXFET.

### 5.1.2 PowerMESH™

The highest rated voltage for power MOSFETs that is currently commercially available is the 1500 V PowerMESH™ from STMicroelectronics. Cryogenic behaviour of such high voltage rated power MOSFETs has not been found in any literature. The fabrication process of the PowerMESH uses a square shaped cellular structure utilising the MESH OVERLAY™ process, which has been applied in other devices such as IGBTs. Since it is a very high voltage power MOSFET, following the theory discussed in Fig. 3.17(a), the dopant concentration of the drift region would be approximately  $1 \times 10^{14} \text{ cm}^{-3}$ . A 1500 V rated PowerMESH (4 A, STP4N150, in TO-220 package) was measured at 294 K, 250 K, 200 K, 150 K, 100 K, 75 K, 50 K and 20 K. The gate voltage was set at 15 V. The breakdown behaviour measurement was not conducted since the required voltage was higher than the rated level of all the interconnection within the cryogenic rig.

The forward IV characteristics of the measured PowerMESH are presented in Fig. 5.12. The measurements at 50 K and 20 K are highlighted with blue and red to differentiate from the higher temperature measurements. The on-state behaviour improved dramatically as temperature was reduced from room temperature to 75 K. Degradation was observed at 50 K but was still comparable to the device behaviour at 100 K. However, at 20 K, the device characteristic became worse than the room temperature measurement. At 20 K, it also exhibited similar non-ohmic behaviour as seen in measurements the HEXFETs. The extracted on-state resistances are presented in Fig. 5.13(a). It was 14.7 times lower at 75 K than room temperature.

The reverse body diode characteristics were also measured and presented in Fig. 5.13(b).

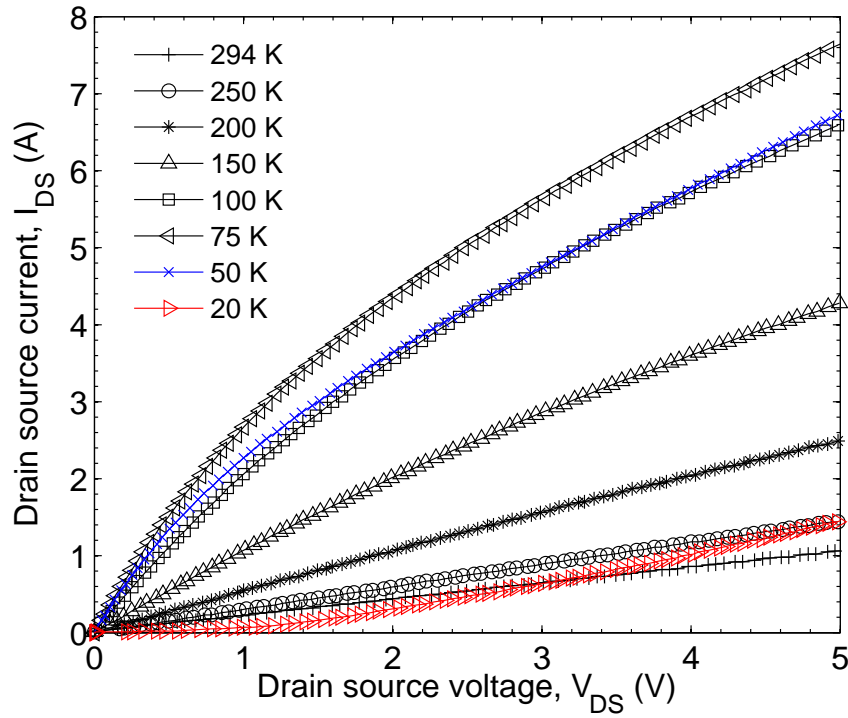


Figure 5.12: The measured forward IV characteristics of a 1500 V PowerMESH™ at  $V_{GS}=15$  V.

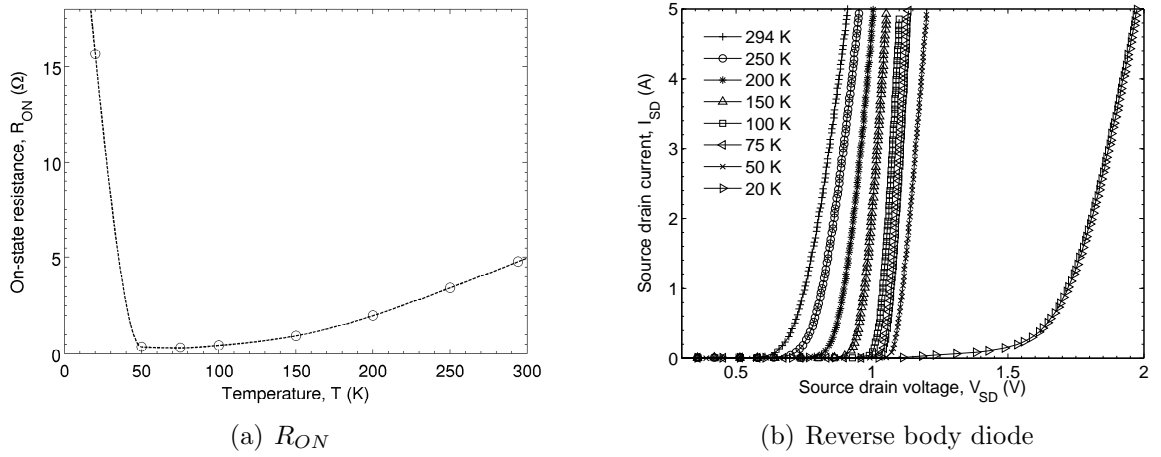


Figure 5.13: The extracted (a) on-state resistance at  $V_{GS}=15$  V and (b) the measured reverse body diode characteristics of a 1500 V PowerMESH™.

The diode turn-on voltage increased in a steady manner at lower temperatures but saturates below 100 K. At 20 K, the diode was  $\sim 0.6$  V higher than at 50 K. This is a sudden sharp

increase when compared to the rest of the trend. However, there is weak conduction from 1 V to 5 V which means the device is actually turned on at around 1 V but only fully turned-on above 1.5 V. Similar behaviour was observed for the p-channel HEXFETs and the forward threshold voltage of IGBTs in [42].

### 5.1.3 Super-junction MOSFETs

As introduced in Chapter 2.1, SJ MOSFETs have superior properties when compared with conventional power MOSFETs. This is due to their alternating P and N pillars structure in the drift region. This enables the use of a higher doped drift region compared to the conventional limits of silicon for the same breakdown voltage capability. Schlogl et al. have claimed that the CoolMOS™ device from Infineon is the ideal device for cryogenic applications down to 77 K and they have characterised a 600 V CoolMOS down to 80 K [36]. Here, SJ devices such as CoolMOS and semi-SJ device such as MDMesh™ will be measured down to 20 K to understand whether the benefits of SJ MOSFETs are still applicable below 80 K.

#### 5.1.3.1 CoolMOS™

The CoolMOS structure is basically identical to the device structure presented in Fig. 2.16, the current path through the drift region is narrower compared to conventional structures. However, with the higher dopant concentration and thinner drift region, lower on-state resistance can be achieved. Three samples of the 560 V CoolMOS (rated at 21 A, SPP21N50C3, in TO-220 package) were measured and they are named CoolMOS 1, 2 and 3 for identification purposes. They were characterised at temperatures of 294 K, 250 K, 200 K, 150 K, 100 K, 50 K and 20 K. The three identical CoolMOS devices were compared and their forward IV characteristics at  $V_{GS}=15$  V are shown in Fig. 5.14, as well as their extracted on-state resistance at the same gate voltage. The forward IV characteristics at 50 K and 20 K are highlighted with blue and red respectively to differentiate them from the higher temperature measurements. The three CoolMOS devices exhibited near identical behaviour at temperatures above 100 K with some negligible variations at 200 K and 294 K. However, at temperatures below 100 K, CoolMOS 1 exhibited very little change in on-state resistance.

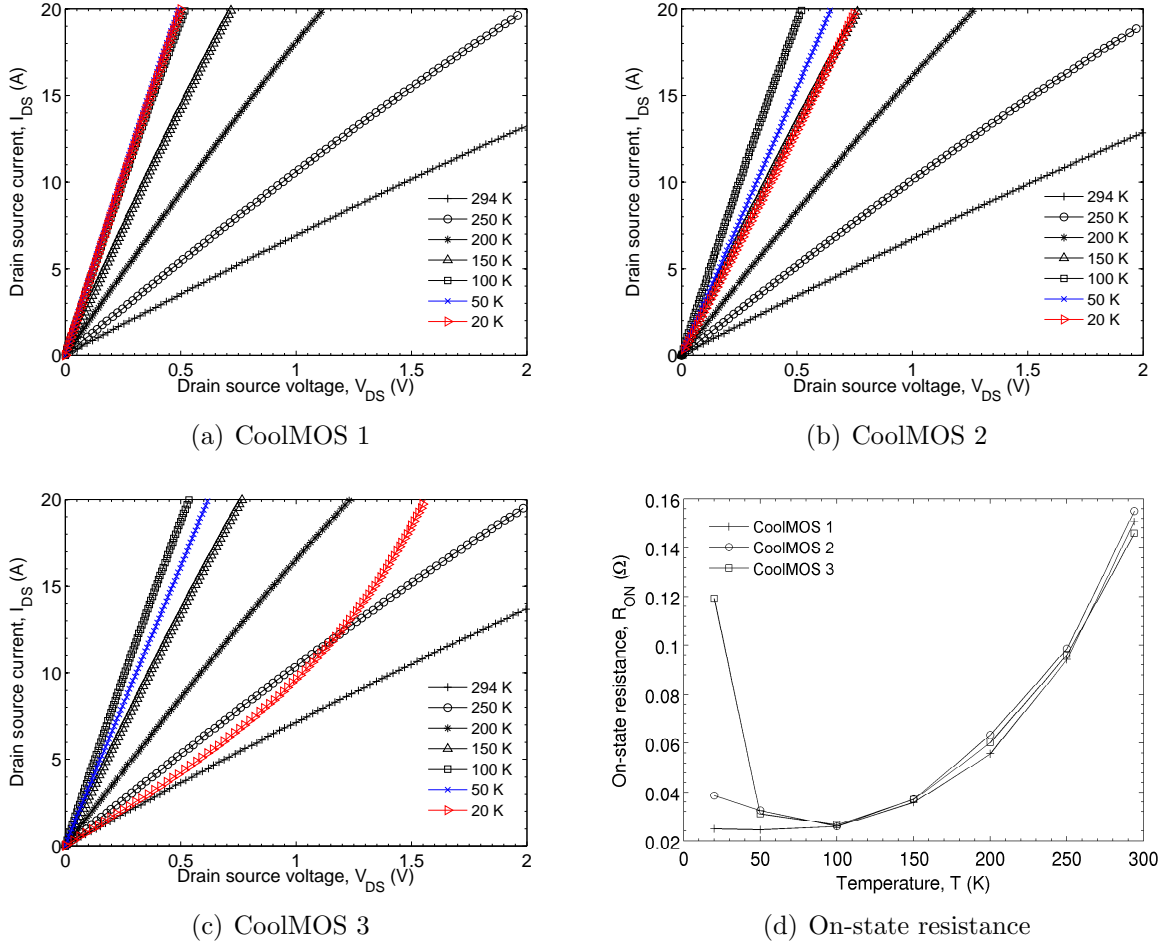


Figure 5.14: (a),(b) and (c) The temperature dependent forward IV characteristics of three CoolMOS devices (SPP21N50C3) and (d) the extracted on-state resistance at  $V_{GS}=15$  V.

Whereas, CoolMOS 2 exhibited a slight degradation at lower temperatures. However, CoolMOS 3 exhibited non-ohmic behaviour at 20 K with serious on-state resistance degradation. On average, the on-state resistance at 100 K was 5.8 times lower than at room temperature.

The IV characteristics of the reverse body diodes of the three CoolMOS devices are presented in Fig. 5.15. The three diodes exhibited close to identical behaviour at temperatures above 100 K. However, at temperatures below 100 K, all three diodes show different characteristics. CoolMOS 1 exhibited little increase in turn-on voltage, whereas CoolMOS 2 exhibited higher turn-on voltage and on-state resistance. At 20 K, the diode showed non-linear IV dependence after turn on with its on-state resistance changing at different current

levels. For CoolMOS 3, this effect is more pronounced, with the 20 K measurement showing much higher voltage drop at higher current levels.

The breakdown voltages of the three CoolMOS devices are presented in Fig. 5.15(d). All three CoolMOS devices exhibited similar temperature dependent characteristics. The breakdown voltages are an average of  $\sim 33\%$  lower at 20 K than at room temperature, with CoolMOS 3 showing a slightly higher reduction at  $\sim 34\%$ .

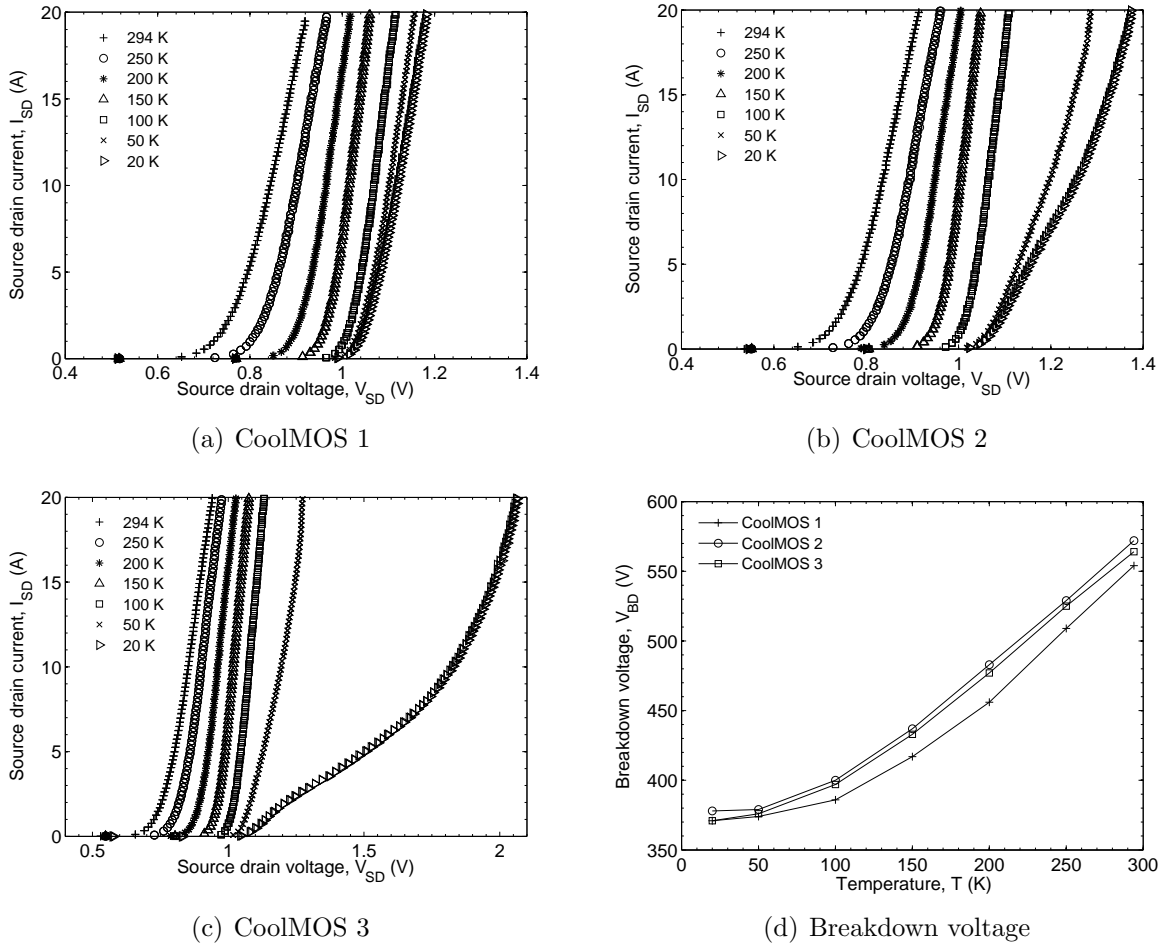


Figure 5.15: (a),(b) and (c) The temperature dependent IV characteristics of the reverse body diodes and (d) breakdown voltages of three 560 V CoolMOS.

### 5.1.3.2 MDMesh™

The MDMesh is another power MOSFET based on the SJ concept from STMicroelectronics. It has a vertical structure similar to that shown in Fig. 2.16. However, the P-type pillars do not reach all the way down to the substrate [33]. This leaves an extra layer of conventional drift region underneath the SJ structure. This makes it effectively a semi-SJ device. Three samples of the 550 V MDMesh device (rated at 20 A, STW20NM50, in TO-247 package) were measured and they have been designated MDMesh 1, 2 and 3 for identification purposes. The three identical MDMesh devices were compared and their forward IV characteristics at  $V_{GS}=15$  V are presented in Fig. 5.16, as well as their extracted on-state resistance at the same gate voltage. The forward IV characteristics at 50 K and 20 K are highlighted with blue and red respectively to differentiate them from other temperature measurements.

As seen by the extracted on-state resistance shown in Fig. 5.16(d), the temperature dependence is not consistent between the three MDMesh devices. However their IV characteristics are fairly similar at temperatures above 50 K. At temperatures below 50 K, all three MDMesh devices exhibited very different IV characteristics. MDMesh 1 exhibited very little change at 20 K, whereas MDMesh 2 exhibited on-state resistance degradation. In addition, MDMesh 3 exhibited non-ohmic behaviour at 20 K, similar to the CoolMOS behaviour. On average, the on-state resistance at 100 K was 6.4 times lower than at room temperature.

The reverse body diode IV characteristics of the three MDMesh devices are presented in Fig. 5.17. The three diodes exhibited near identical behaviour at temperatures above 50 K. However, at 20 K, all three diodes exhibited different characteristics. MDMesh 1 exhibited little increase in on-state resistance, whereas MDMesh 2 exhibited higher on-state resistance. The on-state resistance of MDMesh 3 is even higher than MDMesh 2. However, no non-linear behaviour was observed at the measured current level.

The breakdown voltages of the three MDMesh devices are presented in Fig. 5.17(d), the breakdown voltages were an average of  $\sim 23\%$  lower at 20 K than at room temperature. MDMesh 2 and 3 have similar temperature dependent breakdown voltages. However, MDMesh 1 has a lower breakdown voltage at room temperature than the stated voltage rating.



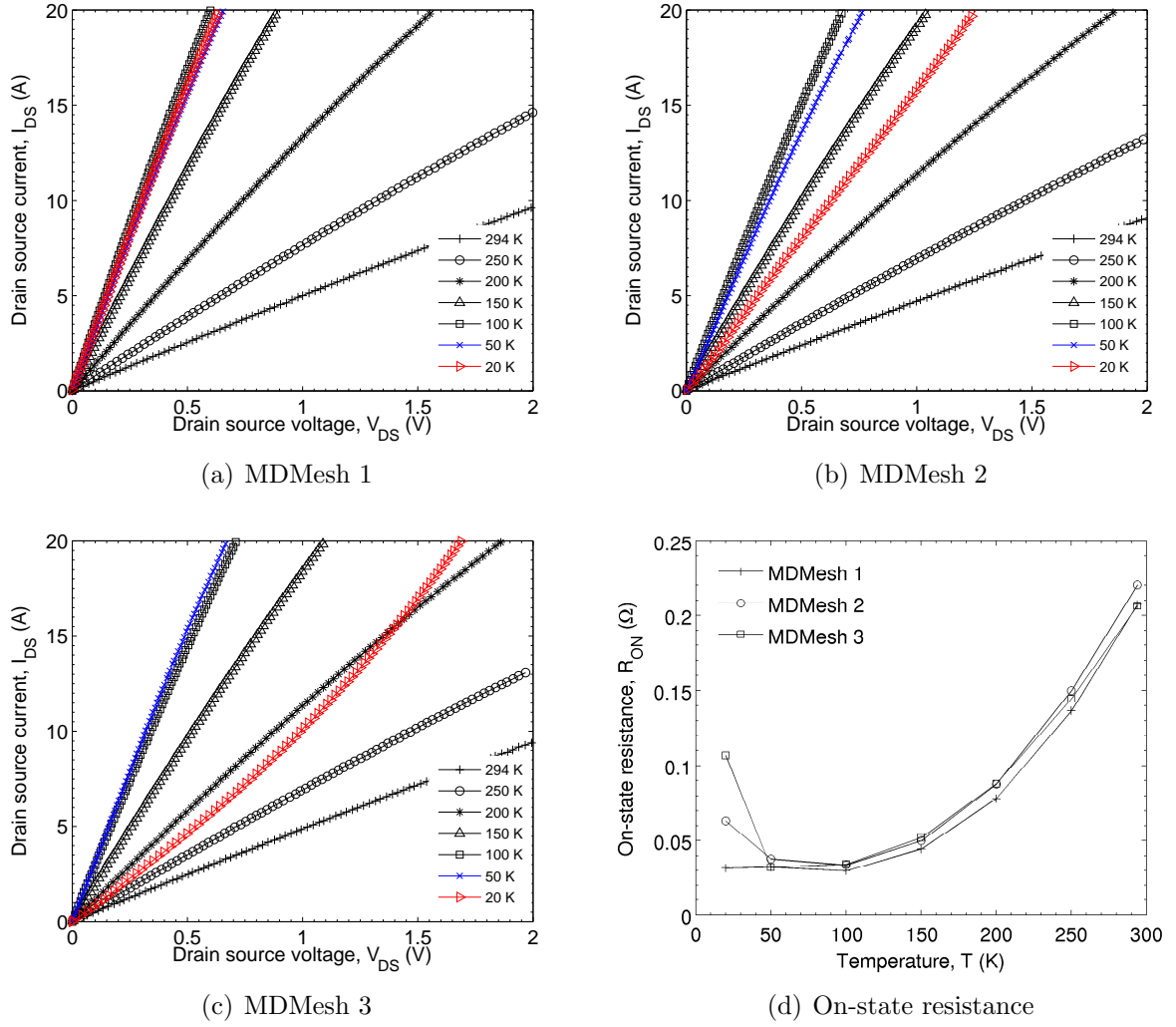


Figure 5.16: (a),(b) and (c) The temperature dependent forward IV characteristics of three MDMesh device (STW20NM50) and (d) the extracted on-state resistance at  $V_{GS}=15$  V.

#### 5.1.4 Comparison between Super-junction MOSFETs and Conventional power MOSFETs

For conventional operating temperatures, SJ MOSFETs such as CoolMOS and MDMesh are known to be superior in terms of achievable on-state resistance at the same breakdown voltages when compared to conventional power MOSFETs such as HEXFETs. However, it is unknown whether this superiority extends down to 20 K. Therefore, in this section a direct comparison between CoolMOS, MDMesh and HEXFET devices of similar voltage and

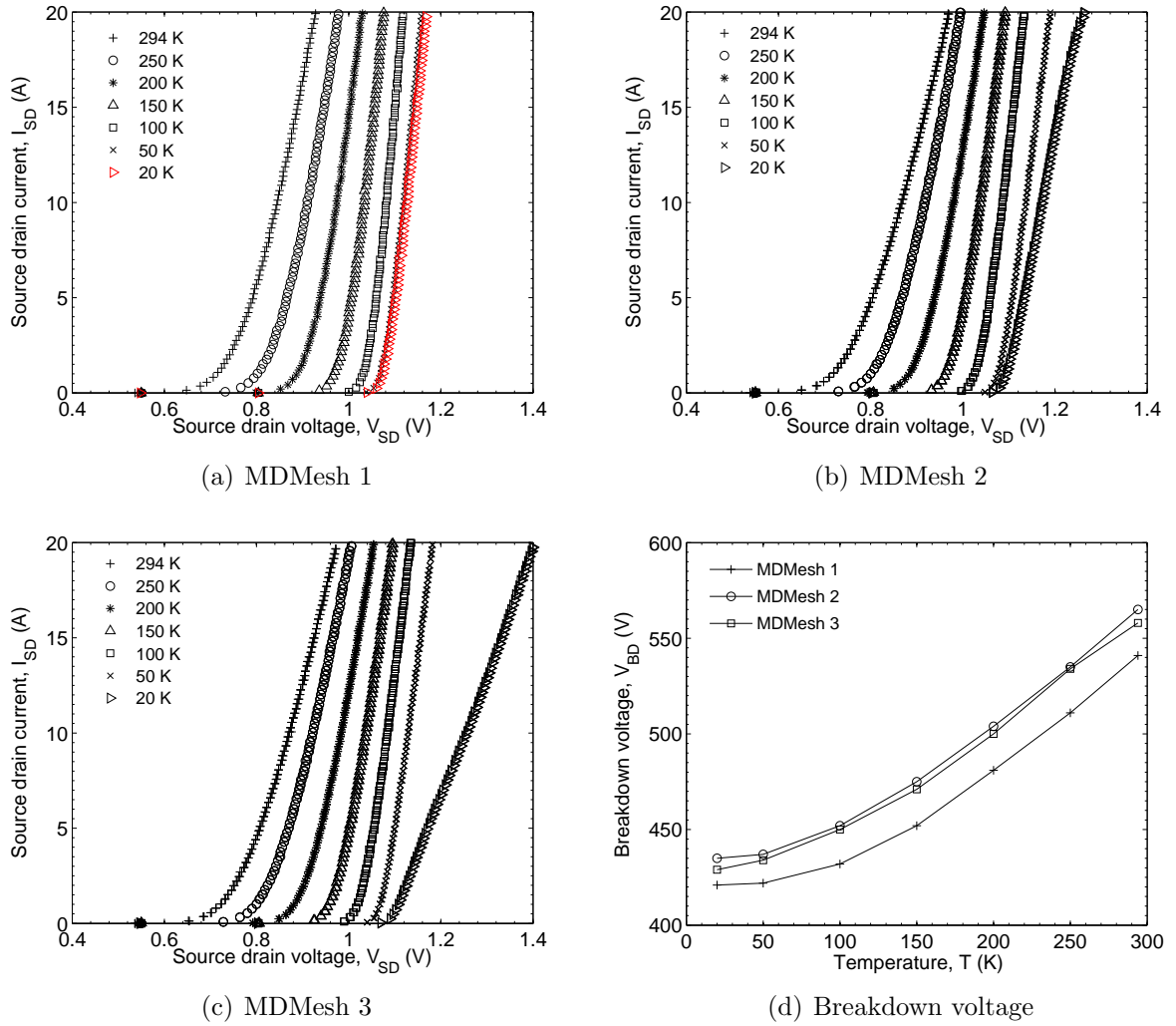


Figure 5.17: (a),(b) and (c) The temperature dependent IV characteristics of the reverse body diode of three MDMesh (STW20NM50) and (d) the breakdown voltages.

current ratings is presented.

#### 5.1.4.1 500 V HEXFET

The closest HEXFET device in terms of similar voltage and current ratings to the two SJ MOSFETs is the 500 V HEXFET (IRFP460, 20 A, TO-247 packaged). Three samples were measured and, for identification purpose, they are designated as HEXFET 1, 2 and 3. The three identical HEXFET devices compared and their forward IV characteristics at  $V_{GS}=15$  V are presented in Fig. 5.18, as well as their extracted on-state resistance at the same gate

voltage. The forward IV characteristics at 20 K are highlighted with red to differentiate them from other temperature measurements.

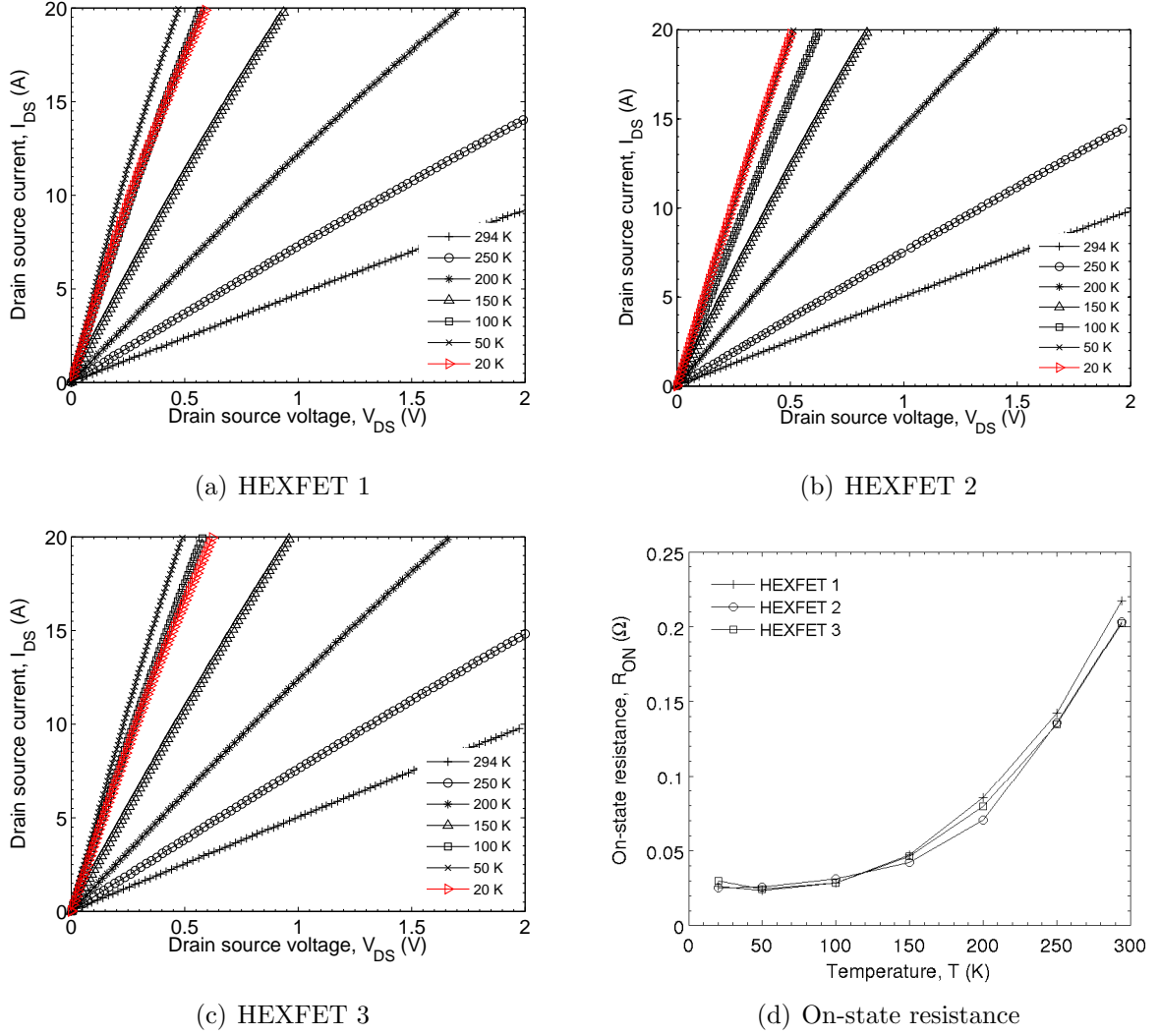


Figure 5.18: (a),(b) and (c) The temperature dependent forward IV characteristics of three HEXFETs (IRFP460) and (d) the extracted on-state resistance at  $V_{GS}=15$  V.

The forward IV characteristics of the three HEXFET devices are fairly similar across the full measured temperature range. With the exception of some slight variation at room temperature and 200 K. At 20 K, HEXFET 1 and 3 exhibited a slight degradation in on-state resistance, whereas HEXFET 2 did not show any noticeable change. Unlike the SJ MOSFETs, variations in the on-state resistance below 50 K were small. Non-ohmic behaviour

was not observed in any of the measured HEXFETs. On average, the on-state resistance was 8.4 times lower at 50 K than at room temperature.

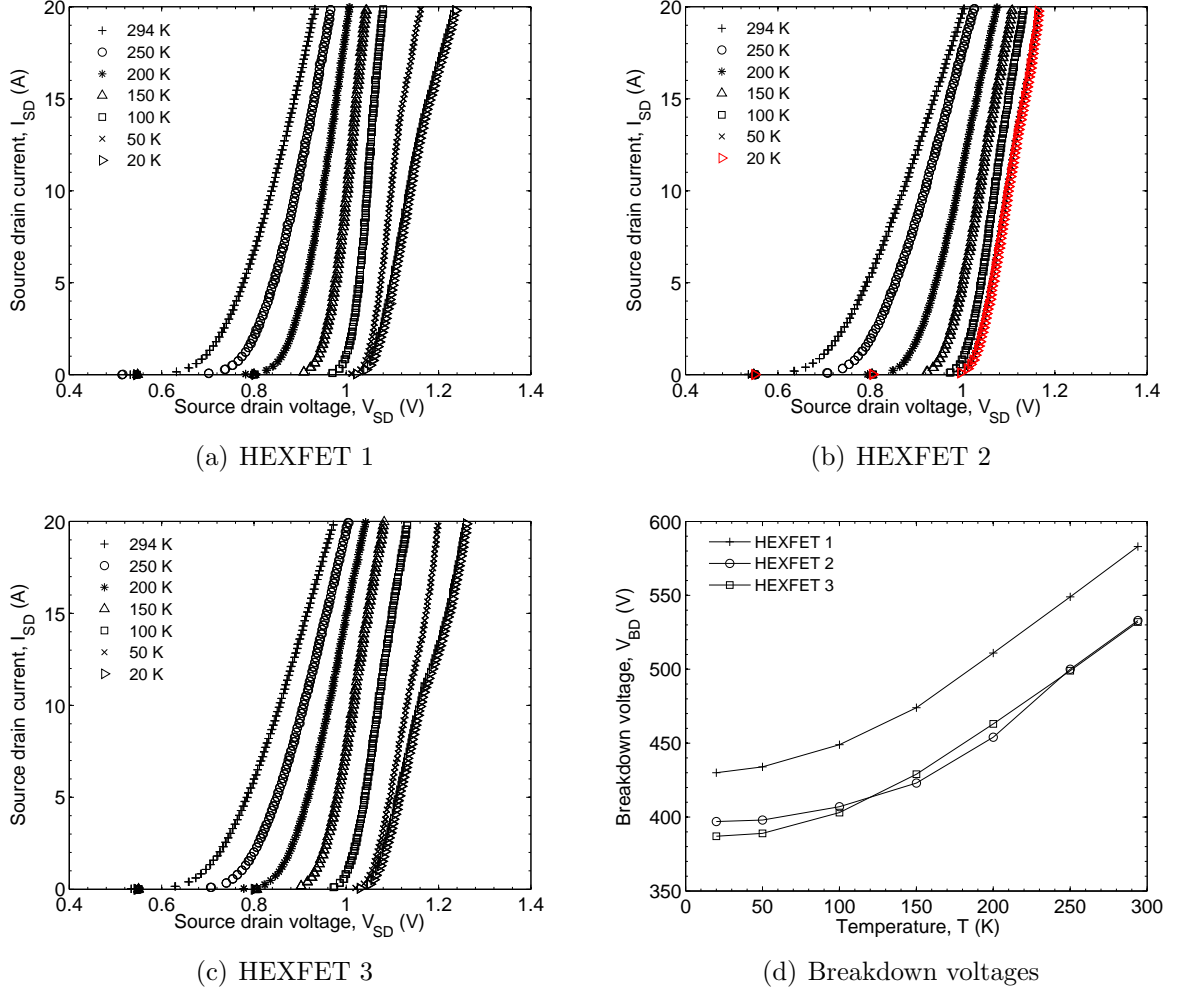


Figure 5.19: (a),(b) and (c) The temperature dependent IV characteristics of the reverse body diode of three HEXFETs (IRFP460) and (d) the breakdown voltages.

The reverse body diode IV characteristics of the three HEXFET devices are presented in Fig. 5.19. All three body diodes exhibited different on-state resistances at room temperature. HEXFET 1 has the lowest on-state resistance, HEXFET 2 has the highest and HEXFET 3 is in between. At temperatures below 50 K, HEXFET 1 and 3 exhibited odd behaviour. They showed a slight increase in on-state resistance when the current increased beyond a certain threshold. For HEXFET 1, this is at  $\sim 15$  A and for HEXFET 3 this is at  $\sim 11$  A. However,

in the same temperature range, HEXFET 2 exhibited no differences between 50 K and 20 K with no observable non-linearity.

The breakdown voltages of the three HEXFET devices are presented in Fig. 5.19(d). The breakdown voltages were an average of  $\sim 26\%$  lower at 20 K than at room temperature. HEXFET 1 and 3 have different breakdown voltages but the shape of their temperature dependence curves are almost identical. HEXFET 2 has the lowest drop in breakdown voltage between room temperature and 20 K.

#### 5.1.4.2 Comparison

The average on-state resistances of the three types of power MOSFET are presented in Fig. 5.20. The error bars show the maximum and minimum value of three identical samples for each type of device. All three power MOSFETs exhibited a global minimum on-state resistance between 50 K and 100 K. Below this range, the decreased electron mobility and carrier freeze-out effect dominates and the average on-state resistances increase. The figure shows that the variations in the on-state resistances for all three power MOSFETs between the samples are small above 100 K. However, at temperatures below 50 K, where the carrier freeze-out effect becomes significant, the variations between different samples increases. This is especially pronounced in the two SJ devices. The most likely reason for this is the stronger carrier freeze-out characteristics for higher dopant concentrations [73]. The range of variation is also much larger; this could be due to minute differences in dopant concentrations between devices from different manufactured batches. Interestingly, both the CoolMOS and MDMesh samples contain one device that was not affected by the carrier freeze-out effect below 50 K.

The average breakdown voltages of the three types of power MOSFET are presented in Fig. 5.21(a). The error bars show the maximum and minimum value of three identical samples for each type of device. Fig. 5.21(b) presents the normalised average breakdown voltage of the three power MOSFETs to room temperature. All three power MOSFETs exhibited a reduction in breakdown voltage with decreasing temperature. However, the CoolMOS devices exhibited the largest drop in breakdown voltage, with the value at 294 K 34% higher than at 20 K. The difference for the HEXFET and MDMesh devices is 26%

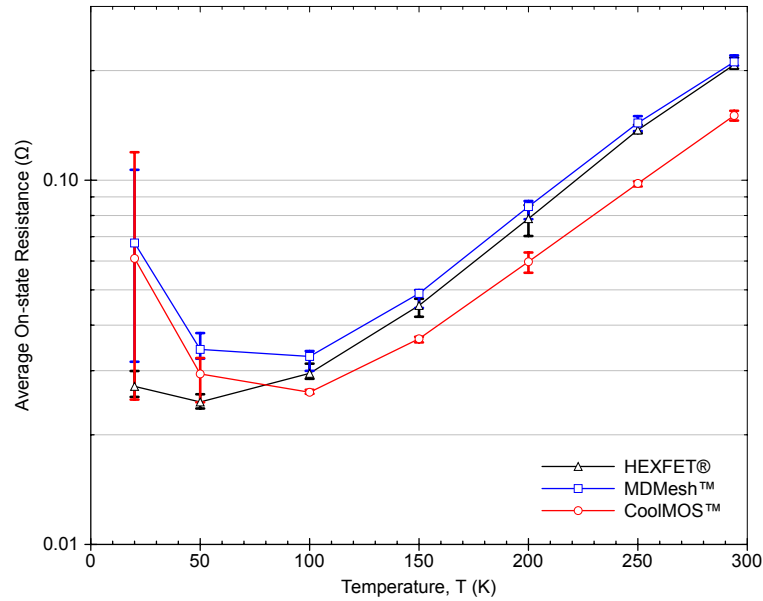


Figure 5.20: The average on-state resistances of the three MOSFETs against temperature. The variation between samples is also presented.

and 23% respectively. The HEXFET shows the biggest range of variation between different samples. There is a 50 V difference between the best and worst samples at 294 K and 43 V at 20 K. This shows that it may be necessary to characterise each device down to the lowest operating temperature before actual operation. Previous literature has assumed that the breakdown voltage is linearly dependent on temperature. However, it is clear from measured data that this linear dependence is not valid below 150 K, as shown in Fig. 5.21(b).

As the breakdown behaviour of power MOSFETs degrades at lower temperatures, it is important for devices operating at low temperatures to be able to sustain the required breakdown voltages. With the on-state resistance improvement down to 50 K, there is a trade-off between the breakdown requirement and on-state resistance. Fig. 5.22 presents the trade-off between the breakdown voltage and the on-state resistance for the three power MOSFETs at 294 K, 150 K and 20 K. The ideal results would be positioned at the bottom right side of the graph, where a device can sustain high voltages and achieve a low on-state resistance. At room temperature, the CoolMOS is by far the best device of the three, achieving both the highest breakdown voltage and lowest on-state resistance. At 150 K, the on-state resistances of all three power MOSFETs are similar and the MDMesh sustains

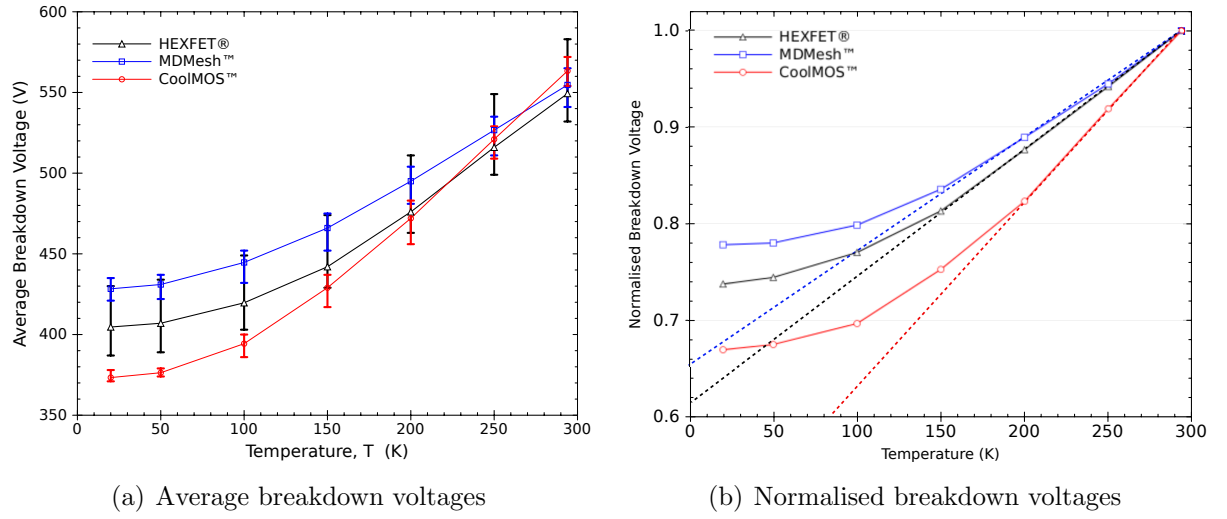


Figure 5.21: (a) The average breakdown voltages of HEXFET®<sup>®</sup>, MDMesh™ and CoolMOS™ from 294 K down to 20 K and (b) the normalised breakdown voltages to 294 K from part (a).

the highest breakdown voltage. At 20 K, CoolMOS has the lowest breakdown voltage and HEXFET achieves the lowest on-state resistance. Therefore, in order to operate these devices at cryogenic temperatures, selecting the best power MOSFET will depend on the specific

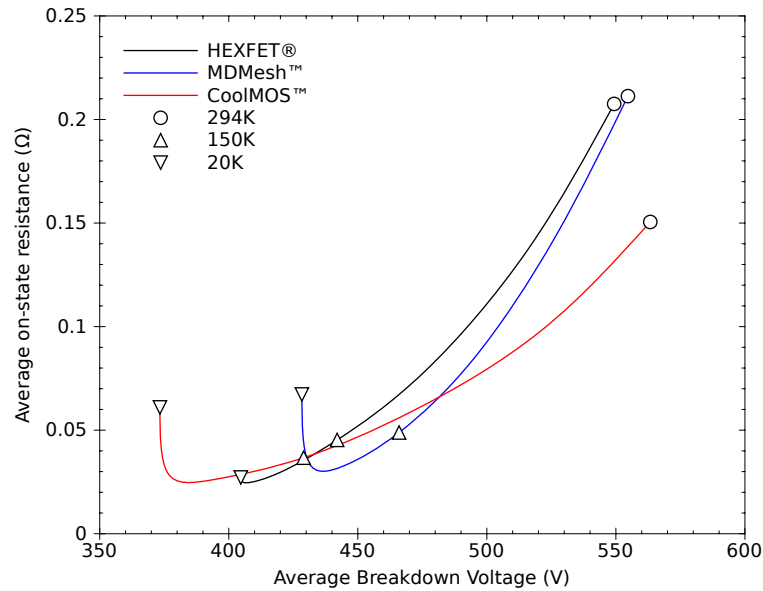


Figure 5.22: Average on-state resistance against average breakdown voltage at different temperatures.

requirements of the application: the operational temperature range, breakdown voltage and maximum power losses.

### 5.1.5 Silicon Carbide MOSFETs

Recent progress in silicon carbide processing techniques have led to the commercialisation of silicon carbide MOSFETs [100]. However, most silicon carbide MOSFETs are still in the prototype stage, mainly due to reliability issues with the oxide interface [101]. A prototype sample of a 1200 V SiC power MOSFET (GE12N152) from GE was measured down to 20 K. The device has an estimated rated current of 25 A. To the knowledge of the author, no cryogenic data of SiC MOSFETs has previously been published.

The temperature dependent forward IV characteristics of the measured SiC MOSFET are presented in Fig. 5.23. The figures present the measured data at  $V_{GS} = 15, 20$  and  $25$  V. Unlike Si MOSFETs, SiC MOSFET exhibited no improvements at lower temperatures. The extracted on-state resistances for each of the gate voltages are presented in Fig. 5.23(d). The on-state resistance of the linear region exhibited negative temperature dependence down to 50 K. The reason behind this behaviour could be due to a combination of factors, first being the carrier freeze-out effect of SiC at lower temperatures [58]. The second and likely the dominating factor is the large increase in gate threshold voltage which has been discussed by Matocha and Tilak [101]. At 20 K, the on-state resistance appears to decrease slightly compare to 50 K, which means the temperature dependence is non-isotropic below 100 K. Non-ohmic behaviour was also observed at 100 K and below.

The temperature dependent IV characteristics of the reverse body diode of the SiC MOSFET are presented in Fig. 5.23(e). The turn-on voltage was  $\sim 2.5$  times higher at 20 K than at room temperature. Interestingly, the on-state resistance of the body diode remained relatively similar at all the measured temperatures.



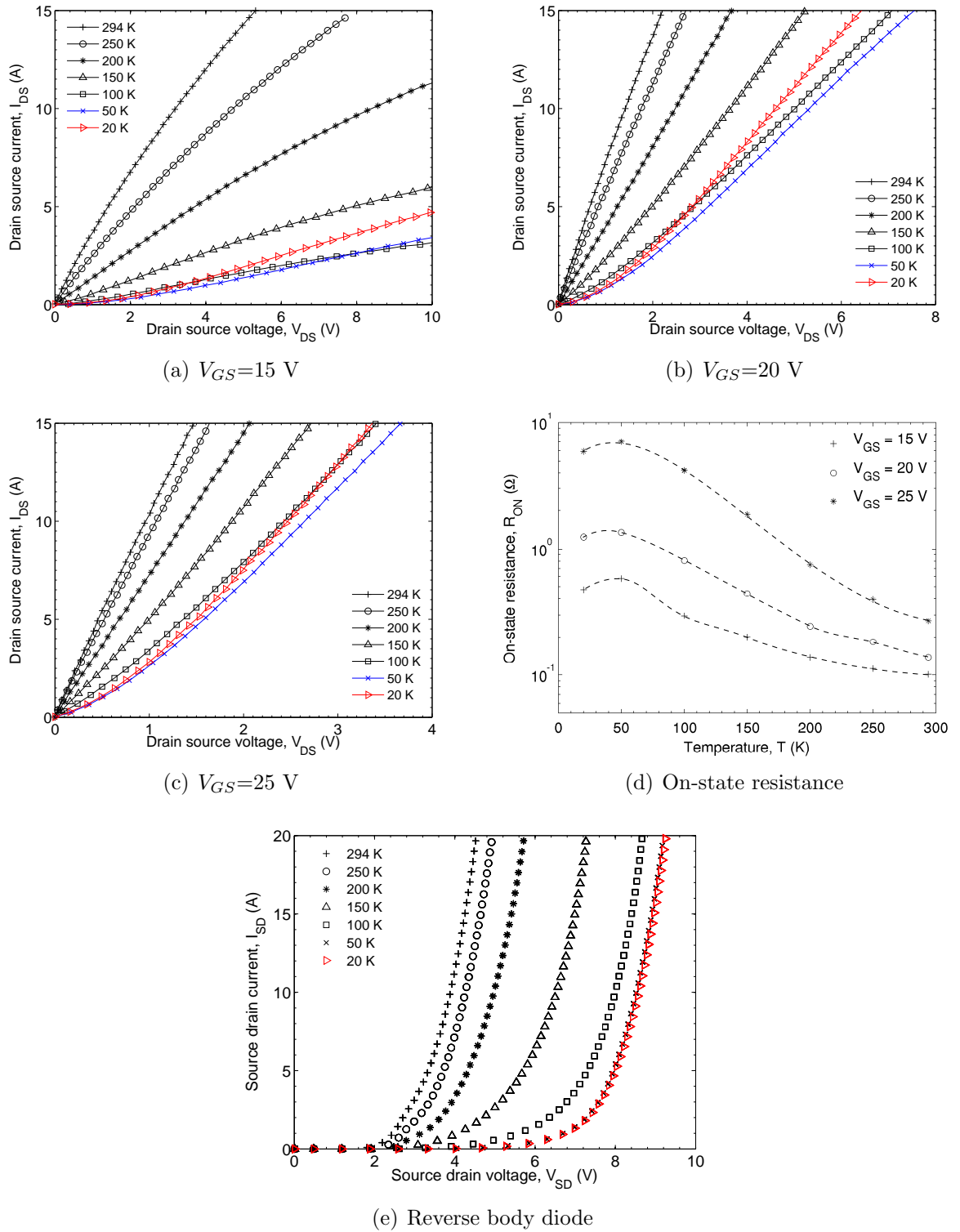


Figure 5.23: The temperature dependent forward IV characteristics of a 1200 V SiC power MOSFET (GE12N152) at (a)  $V_{GS}=15$  V, (b)  $V_{GS}=20$  V, (c)  $V_{GS}=25$  V, (d) the extracted on-state resistance at different gate voltages and (e) the IV characteristics of the reverse body diode.

## 5.2 HEMT

As introduced in chapter 2.3.2, the gallium nitride HEMT has recently been recognized as a viable device for power electronic applications. Previously, HEMT devices were commonly made from gallium arsenide and mainly used in communication applications due their high speed and low noise switching capabilities. However, GaAs HEMTs are fairly low power devices with low rated breakdown voltages. The GaN HEMT has the potential to achieve low on-state resistance as well as high breakdown voltage due to its high critical electric field attributes (See Table. 2.1).

### 5.2.1 GaN HEMT

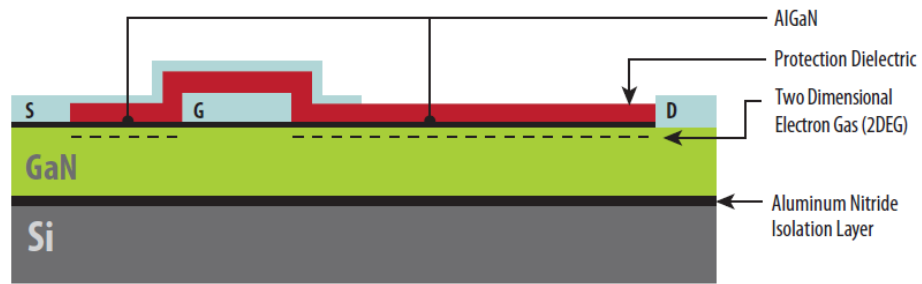


Figure 5.24: The EPC GaN enhancement mode HEMT structure [102].

Currently, GaN HEMTs are still an immature technology. However, a few companies have commercialised some GaN HEMT devices. Efficient Power Conversion (EPC) has introduced an enhancement mode GaN HEMT (Normally off device). These devices are packaged in passivated die form (Flip chip technology) with solder bumps as terminals, hence they are currently only available as surface mount packages. Fig. 5.24 presents the known device structure of the GaN enhancement mode HEMT. It is a lateral device with the active GaN layer grown on a silicon wafer with aluminium nitride used as an isolation layer. The EPC enhancement mode HEMT was designed to behave like a conventional power MOSFET, with a required minimum gate bias to turn on the device. It even has an intrinsic body diode which behaves in a similar manner to the body diode of a power MOSFET but operates via

a different mechanism (unipolar conduction). During reverse bias, with  $V_{GS} = 0$  V, the gate becomes positively biased compare to the drain which turns on the device. This means the GaN HEMT can only block voltage applied at the drain terminal. Unlike the MOSFET, the gate is not isolated from the channel which results in a higher gate leakage. It is also known to have a negative temperature dependence, meaning lower temperature would decrease the gate threshold voltage in contrast to a silicon MOSFET.

A 200 V, 12 A GaN HEMT (EPC1010) was chosen for cryogenic measurement. Due to the bare die form of the device, it was soldered on to a printed circuit board (PCB) to create electrical connections. In order to ensure good thermal conduction, the back of the die is held in thermal contact with the copper cold-head with a thin layer of silicone thermal pad in between, this is illustrated in Fig. 5.25.

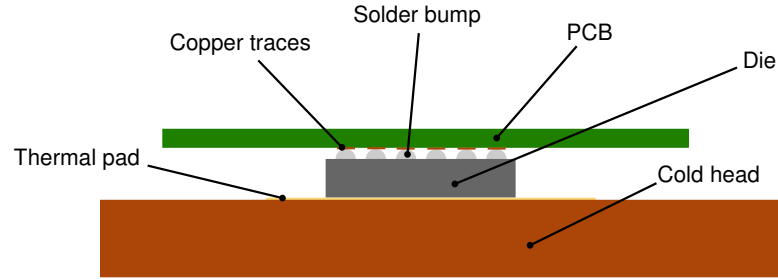


Figure 5.25: The electrical and thermal connections with the GaN die during characterisation.

The temperature dependent forward IV characteristics of the GaN HEMT at  $V_{GS} = 5$  V is presented in Fig. 5.26(a). The device improves at lower temperatures and exhibits no sign of degradation or non-ohmic effects even down to 20 K. This is expected from the temperature independent two dimensional electron gas density of the channel. The extracted on-state resistance is presented in Fig. 5.26(b). The on-state resistance reduces at lower temperatures but appears to saturate at temperatures below 50 K. The on-state resistance is five times higher at room temperature than at 20 K, However this includes the measurement errors from the additional resistance caused by the PCB connections. The measured gate threshold voltage of the device is presented in Fig. 5.26(c). As expected, the gate threshold voltage decreased with decreasing temperature; from  $\sim 1.3$  V at room temperature down to  $\sim 0.25$  V

at 20 K. The same effect occurs in MOSFETs at high temperature. It is important to note that at such low gate threshold voltage, there is a real danger of parasitic turn-on from voltage spikes or even noise on the gate terminal. Although such effects are generally mitigated at cryogenic temperatures.

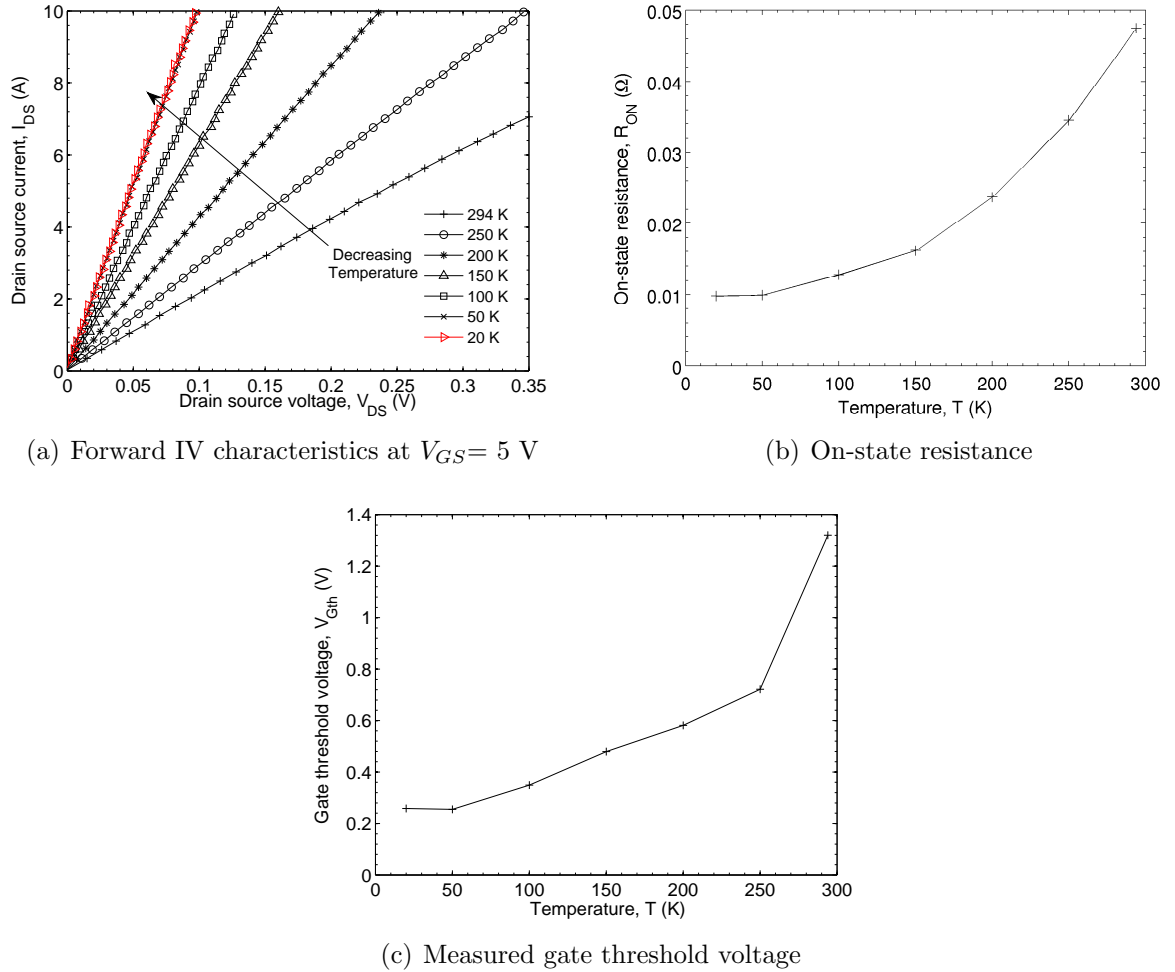


Figure 5.26: The temperature dependent (a) forward IV characteristics at  $V_{GS} = 5$  V, (b) the extracted on-state resistance and (c) the measured gate threshold voltages.

The temperature dependent IV characteristics of the reverse Schottky diode are presented in Fig. 5.27(a). The turn-on voltage of the Schottky diode followed a similar negative temperature dependence to the gate threshold voltage. The diode turn-on voltage saturates at temperatures below 100 K. It also exhibits negative resistance when the current rises be-

yond  $\sim 2$  A. Fig. 5.27(b) presents the measured temperature dependent breakdown voltage taken at  $I_{SD} \simeq 250 \mu A$ . The breakdown voltage is  $\sim 34\%$  lower at 20 K compared to room temperature. The breakdown voltage at room temperature was lower than the rated breakdown voltage which means the device could have degraded during the soldering process. The breakdown voltage at 100 K was higher than expected from the trend of the temperature curve. This could be due to a measurement error.

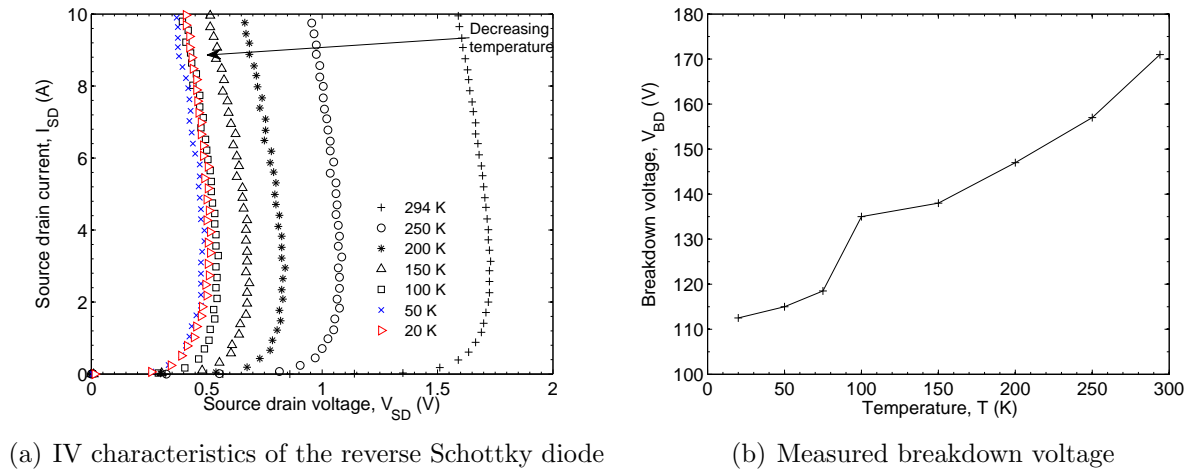


Figure 5.27: The temperature dependent (a) IV characteristics of the reverse Schottky diode and (b) the measured breakdown voltages.

## 5.3 Power Schottky Diodes

Power Schottky diodes have the potential to achieve lower power loss than PiN diodes at cryogenic temperatures. This is because the conductivity of the diode is dependent on unipolar conduction which improves at lower temperatures. The turn-on voltage of the Schottky diode is also lower than the turn-on voltage of the PiN diode which would result in a lower voltage drop. Furthermore, the turn-on voltage of a Schottky diode can be controlled by the Schottky barrier height, which is dependent on the metal type, dopant concentration of the semiconductor and interface conditions; all of which can be precisely controlled during fabrication. In terms of the reverse behaviour, edge terminations are commonly added to

improve the breakdown voltage by spreading the electric field so that the junction does not breakdown prematurely, this also reduces the reverse leakage current. However, how this influences the cryogenic behaviour of power Schottky diodes is uncertain since data on their cryogenic behaviour has not been found in any literature. Therefore, it is the aim of this section to present the measured cryogenic behaviour of several silicon power Schottky diodes. The cryogenic behaviour of gallium arsenide and silicon carbide Schottky diodes is also presented.

### 5.3.1 Silicon Schottky Diodes

The temperature dependent behaviour of four commercially available power Schottky diodes was measured, including forward conduction characteristics and breakdown voltages within the temperature range of 294 K and 20 K. Information on the four diodes is shown in Table 5.1. Diode D1-D3 are conventional Schottky rectifiers and Diode D4 is a trench MOS barrier Schottky (TMBS) rectifier.

Table 5.1: Measured power Schottky diodes, all rated at 200 V

Diodes	Part Number	Manufacturer	Maximum average forward current (A)	Packaging
D1	MBR20200CT	ON Semiconductor	10	TO-220AB
D2	MBR10200CT	SPC Multicomp	5	TO-220AB
D3	DSA90C200HB	IXYS	45	TO-247AD
D4	V302200C	VISHAY	15	TO-220AB

The low current measurements of the forward bias behaviour of D1 are presented in Fig. 5.28. As temperature decreases, the data follows the expected behaviour described by the Schottky diode equation:

$$J_F = J_S \left( \exp \left( \frac{qV}{kT} \right) - 1 \right), \quad (5.1)$$

where  $J_F$  is the forward current density and  $J_S$  is specified in Eqn. 2.3. Interestingly, the data also indicates the formation of a current plateau at 200 K, with this behaviour

becoming more pronounced at lower temperatures. A similar behaviour was also observed in SiC Schottky diodes [59], and barrier inhomogeneity was proposed as the cause for this effect.

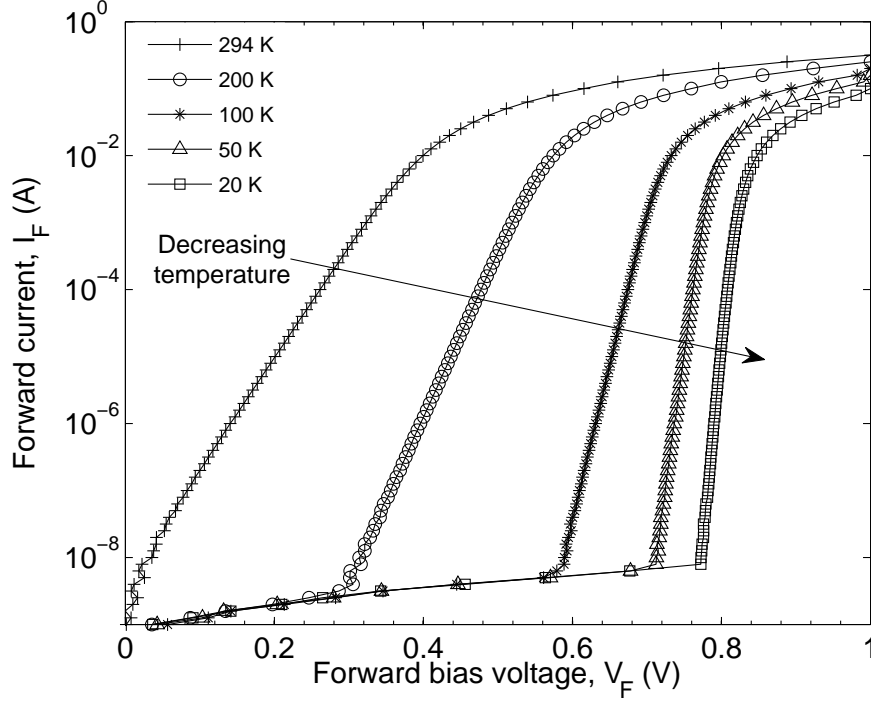


Figure 5.28: Low current-voltage characteristics of D1 at various temperatures.

The forward IV characteristics of D1-D4 with temperature are presented in Fig. 5.29, up to  $I_F=10$  A. The measurements at 20 K are highlighted with red to differentiate them from higher temperature measurements. At room temperature, all four diodes exhibited similar behaviour with small differences in turn-on voltages. All the diodes begin to conduct at around 0.4 V but do not fully turn on until  $V_F \simeq 0.7$  V. This behaviour suggests that these diodes may be conducting via the P+ guard rings in their structures. The P+ guard rings are likely to overlap with the metal contacts which result in PN junctions in parallel with the Schottky junctions, effectively forming a Merged PiN Schottky (MPS) diode, see Fig. 2.9(b). The PN junction has a turn-on voltage that is higher than the Schottky turn-on voltage. Therefore, conduction first occurs in the Schottky region of the device and then through the PN junction regions when the voltage reaches the PN junction turn-on voltage.

This effect is present in all 4 diodes.

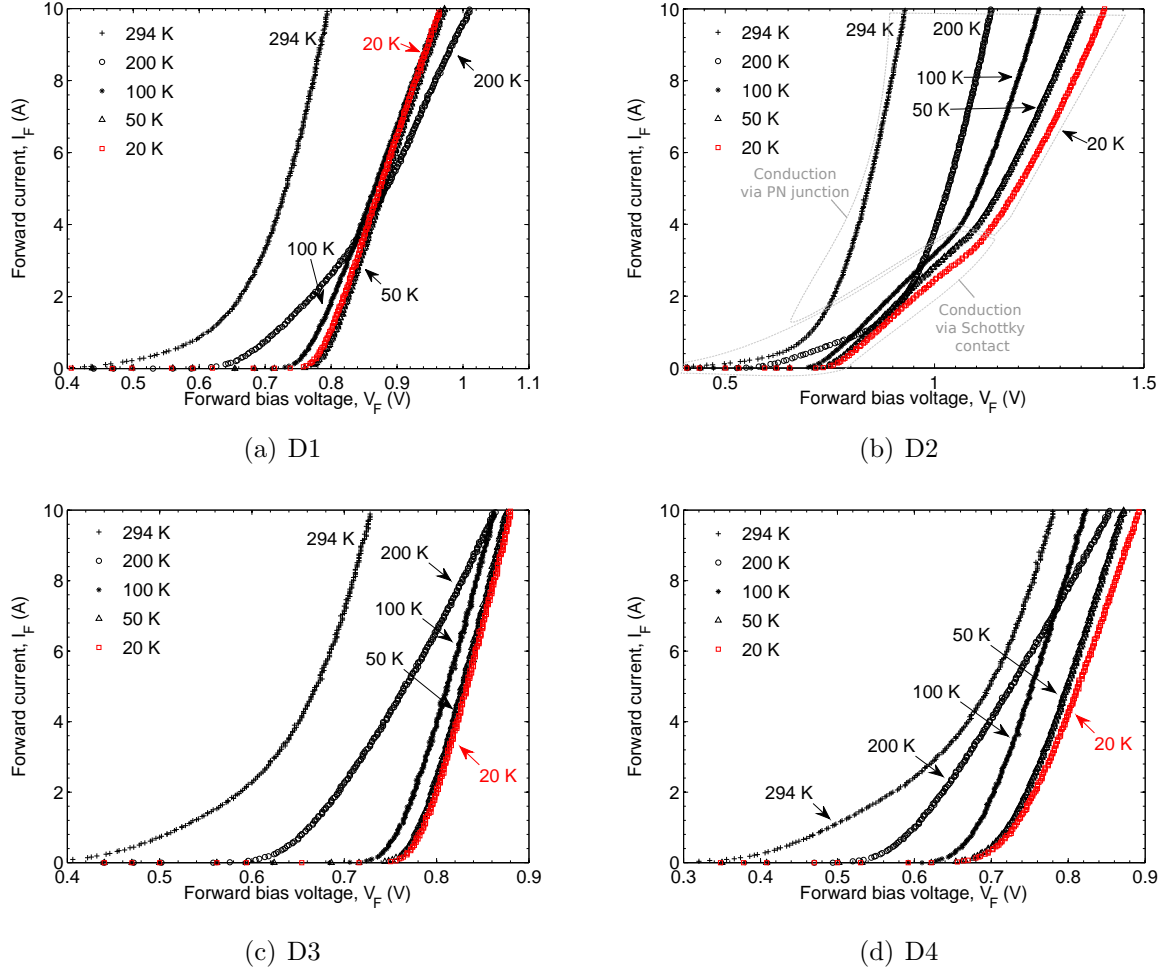


Figure 5.29: The forward IV characteristics of D1-D4 at various temperatures.

The MPS behaviour was observed in all four diodes but the changes of their IV characteristics with temperature are quite different. For D1, conduction through the PN junctions become less apparent at lower temperatures due to their higher turn-on voltage. Therefore, conduction through the Schottky regions begin to dominate. For the measured 294 K and 200 K curves, conduction through the PN junctions can be seen by the increasing IV slope with higher  $V_F$ . However, at temperatures below 100 K, conduction only occurs via the Schottky regions for the presented current range ( $I_F \leq 10$  A). This is mainly due to the increased electron mobility which reduces the resistance of the drift region. This leads to an



over all lower voltage across the device. In this case, the voltage is not high enough to reach the increased turn-on voltage of the PN junction at temperatures below 100 K. Abnormal behaviour was observed at 20 K where the turn-on knee voltage decreased by  $\sim 0.01\text{V}$  when compared to the turn-on knee voltage at 50 K. The measurement was repeated on more than one device and the same behaviour was observed. The reason for this behaviour is unclear.

For D2, conduction via the PN junctions appears to occur even down to 20 K. This is probably due to the higher resistance encountered by the current while conducting via the Schottky regions. There are a number of factors that could cause this, one of the most likely factor is P+ guard rings that extends deeper into the drift region. This creates a type of JFET effect, limiting the current flow via the Schottky junctions. In Fig. 5.29(b), the regions where the different conduction mechanism operate have been indicated. The on-state resistance due to conductivity modulation increases with decreasing temperatures due to the carrier freeze-out effect.

For D3, conduction via the PN junctions appears to occur only in the 294 K curve. This means that for the presented current range ( $I_F \leq 10\text{ A}$ ), due to the low resistance of the device, the voltage across the diode is not high enough to reach the turn-on voltage of the PN junctions.

The behaviour of D4 (TMBS diode) at 294 K suggests that P+ guard rings are also present within the structure. The low temperature behaviour is fairly similar to D3. The Schottky barrier appears to be lowest compared to the other three diodes, hence the low turn-on knee voltage at 20 K. For temperatures below 100 K, the shape of the knee curves of D4 appears to be more rounded when compared to the other diodes, where the knee curves are more abrupt. This suggests that additional conduction mechanisms may be involved.

The on-state resistance at 8 A of the four diodes are further illustrated in Fig. 5.30(a). The non-isotropic behaviour of D1, D3 and D4 indicate a different conduction mechanism dominates below 200 K. Whereas for D2, the degradation continues down to 20 K similar to a bipolar device.

The temperature dependent breakdown voltages of the four diodes are shown in Fig. 5.30(b). At room temperature, D1, D2 and D4 have breakdown voltages above 200 V,

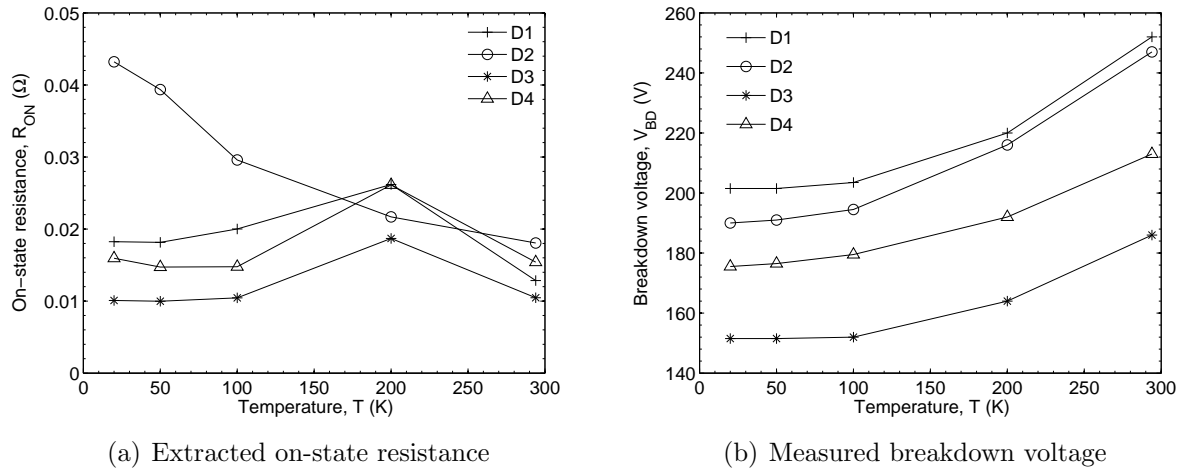


Figure 5.30: (a) The extracted on-state resistance and (b) the breakdown voltages of D1-D4.

however D3 was measured to have a breakdown voltage of 186 V. All four diodes have shown similar temperature dependent breakdown voltage down to 20 K. These curves saturate at temperatures below 100 K. The average breakdown voltage was 20% lower at 20 K than at room temperature.

It is important to note that the conduction losses in all the measured diodes do not decrease at cryogenic temperatures. This is mainly due to the domination of unipolar action at cryogenic temperatures and the bipolar action at room temperature. If the P+ guard rings were to be absent in the structures, conductivity modulation would not occur and therefore the big improvement in electron mobility would be more apparent. On the other hand, the breakdown behaviour would be soft, similar to that seen in planar Schottky diodes. In terms of conduction losses, it is clear that the bipolar conduction at room temperature has a lower power loss compared to unipolar conduction at cryogenic temperatures. This is due to the increased PN junction turn-on voltage at lower temperatures.

### 5.3.2 GaAs Schottky Diodes

For the reasons discussed in chapter 2.3.2, there are virtually no GaAs devices aimed at high power electronics applications. However, there are plenty of GaAs devices aimed at radio

frequency (RF) and high speed switching applications. Some of these devices have power ratings similar to low power devices, therefore a 250 V GaAs Schottky diode (GS150TA25104, 4 A, in surface mount package) by IXYS was selected for cryogenic characterisation. The device has three diodes in parallel with joined connections at the anode terminals, only one of these diodes was connected during the characterisation.

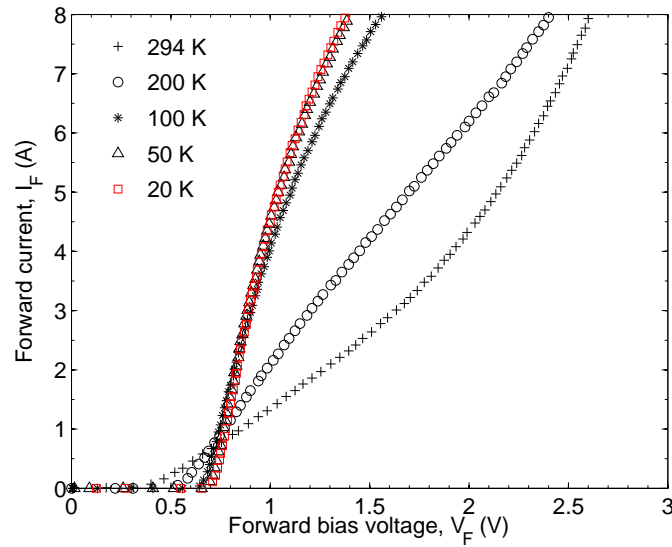


Figure 5.31: The measured forward IV characteristics of the GaAs (GS150TA25104) Schottky diode.

The measured forward IV characteristics of the GaAs Schottky diode is presented in Fig. 5.31 and the data at 20 K is highlighted with red to differentiate it from higher temperature measurements. The data shows the behaviour of the diode at more than twice its rated current. Below the diode's rated current of 4 A, the measured behaviour exhibits increased turn-on voltages and reduced on-state resistance as temperature decreases. This is the expected behaviour of a Schottky diode. The turn-on voltage at 20 K is slightly lower than the measured silicon Schottky diodes. This suggests that the Schottky barrier height is lower than the Si Schottky diodes measured in the previous section. The on-state resistance is 6.4 times lower at 20 K compared to at room temperature. It is also important to note that when  $I_F$  is below  $\sim 0.8$  A, the conduction loss is lower at high temperatures than at lower temperatures due to the increases in turn-on voltage. As this device is only rated at 4 A,

this means that operating at current levels below 20% of the rated current would give no conduction loss improvements at lower temperatures. The behaviour above the diode's rated current is surprisingly different. At temperatures above 200 K, the resistances reduce as the applied voltage increases. This suggests that P+ guard rings might have been used, similar to the Si Schottky diodes in the previous section. However, it does not turn on until the forward bias voltage reaches  $\sim 2$  V. At temperatures below 200 K, the opposite behaviour occurs; the resistances increase at higher applied voltages.

The reverse breakdown IV characteristics of the GaAs Schottky at 294 K, 150 K and 20 K are presented in Fig. 5.32. At 294 K, the curve shows three different stages of reverse conduction at  $\sim 125$  V,  $\sim 225$  V and  $\sim 270$  V. The exact breakdown voltage at the temperatures of 150 K and 20 K are difficult to pinpoint due to the abnormal shape of the breakdown curves; however, it is clear that the decrease in breakdown voltage is much higher than in the Si Schottky diodes, around 50-60% between room temperature and 20 K.

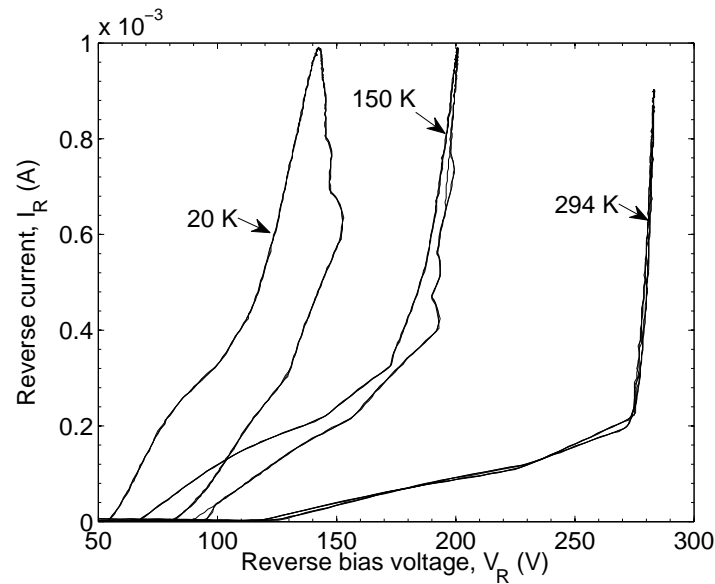


Figure 5.32: The reverse breakdown IV characteristics of the GaAs Schottky at 294 K, 150 K and 20 K.

### 5.3.3 SiC Schottky Diodes

Unlike the SiC power MOSFET, SiC Schottky diodes are relatively easy to fabricate and therefore have been commercially available for a number of years. SiC Schottky diodes have the benefit of fast switching speeds and lower switching losses. They can also sustain much higher breakdown voltages than Si Schottky diodes. A 600 V 4H SiC Schottky diode (C3D06060A, 6 A, TO-220 packaged) by CREE, was selected for cryogenic characterisation.

The measured forward IV characteristics of the SiC Schottky diode up to 10 A are presented in Fig. 5.33. At cryogenic temperatures of 50 K and 20 K, the Schottky diode appears to conduct via the the P+ guard rings once the forward bias voltage reaches the turn-on voltage of the PN junction ( $\sim 3$  V for 4H SiC at room temperature) [103], this behaviour is similar to the previously measured Si Schottky diodes. Between room temperature and 100 K, the SiC Schottky diode appears to conduct via the Schottky junction only. Interestingly, the on-state resistance reduced as temperature reduced from room temperature down to 200 K but increase drastically below 200 K.

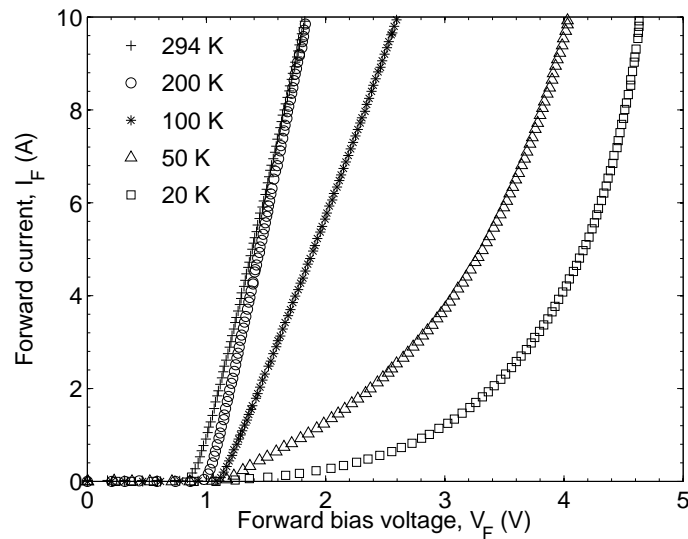


Figure 5.33: The measured forward IV characteristics of the SiC (C3D06060A) Schottky diode.

The temperature dependent breakdown voltage of the SiC Schottky diode is presented in Fig. 5.34, the breakdown voltage was taken at a reverse current of  $250 \mu\text{A}$ . From 294 K

to 150 K, the breakdown voltage decreased in a linear fashion, similar to the temperature dependence of Si diodes over the same temperature range. However, below 150 K, the breakdown voltages exhibited non-monotonic behaviour. The breakdown voltage increased slightly from 150 K down to 75 K and decreased at temperatures below, showing a local maximum at around 75 K.

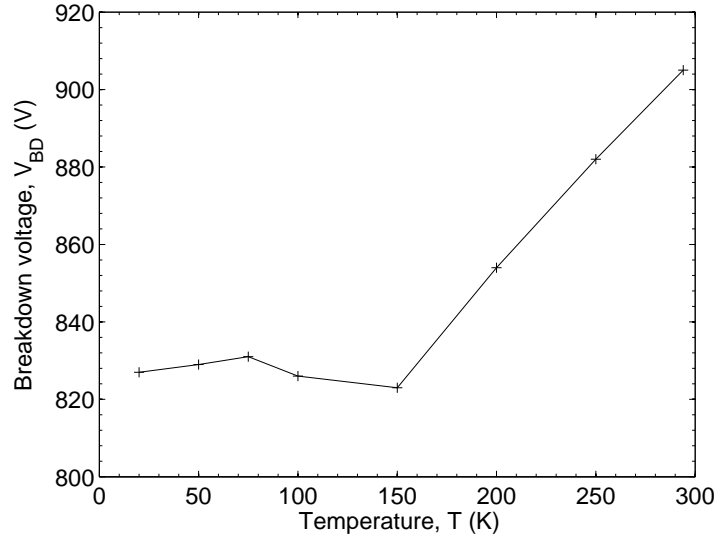


Figure 5.34: The temperature dependent breakdown voltage of the SiC Schottky diode.

## 5.4 Device Package Observations

For each of the device characterisations, the device under test was subjected to cryogenic conditions for between six and nine hours, with further warm up which last for at least 24 hours (to slowly bring the device from cryogenic temperatures back to room temperature). From external observations, no device package degradation occurred. Furthermore, some measurements were repeated for the same device for a second day in order to investigate whether the device behaviour would change after returning to room temperature. All the second measurements matched fairly well with the first measurements which means the device behaviour remained the same after single large temperature swings. However, the rate of change in temperature in these cases was very slow. Also, due to the limited size of the

cryogenic cold-head, all the measured devices in this chapter are relatively small packaged devices and large power module packages were not measured.

## 5.5 Summary and Conclusion

As stated in chapter 1, the required operating temperature of these power device is at 30 K. However, from chapter 2, we found out that most of the known behaviour of power devices only extends down to 77 K, the temperature of liquid nitrogen. In this chapter, by characterising power devices down to 20 K, a temperature when carrier freeze-out effects are dominant in silicon, the forward behaviour of the power devices under carrier freeze-out can be analysed.

For n-channel power MOSFETs, there is an optimum temperature range where the device experiences a minimum on-state resistance. This is between 60 K and 90 K, centered at around 75 K. At this range the electron mobility is highest and the temperature is not low enough to cause significant carrier freeze-out effects. From room temperature to the optimum temperature range, power MOSFETs with higher voltage ratings show more significant improvements compared to lower voltage devices. For example, the on-state resistance of the 1500 V PowerMESH device, reduced by a factor of 14.7. Whereas the 500 V HEXFET device reduced by a factor of 8.4 and the 200 V HEXFET device reduced by a factor of 3.6.

Below this optimum temperature range, most devices experience degradation in on-state resistance. This could be due to a combination factors including reduced electron mobility and carrier freeze-out effects. Some devices also exhibited additional non-ohmic behaviour where the on-state resistance becomes dependent on the applied drain voltage and the previously Ohmic region becomes non-linear. The behaviour below the optimum temperature range varied widely between supposedly identical devices. The only exception was the 500 V HEXFET, however, this could be due to the low number of samples taken for measurement. More importantly, some devices did not exhibit carrier freeze-out effects and their on-state resistance remained relatively low even down to 20 K. The devices which appear to be unaffected by carrier freeze-out include both conventional and SJ devices. Devices that

degrade below the optimum temperature range will experience negative temperature dependence where increase temperature reduces the on-state resistance. The turn-on voltage of all the measured body diodes increased with decreasing temperature and some also exhibited carrier freeze-out effects at lower temperatures. The difference in the switching behaviour at cryogenic temperatures has been found to be small and can be considered negligible. The temperature dependence of breakdown voltage below 100 K was found to be non-linear and saturated at a higher voltages than previously expected. Overall, n-channel power MOSFETs can operate at cryogenic temperatures reliably down to 50 K. Below this temperature, some devices are not affected by the carrier freeze-out effects. However, in order to identify these devices, each will have to be characterised at cryogenic temperatures. For p-channel HEXFET devices, the optimum temperature range appears to be at a higher temperature than in n-channel devices, centered at around 100 K. Degradation effects can also be seen at temperature as high as 75 K. Overall, the measured p-channel HEXFET devices were found to be inferior to the n-channel HEXFET devices at temperatures below 100 K.

The measured SiC power MOSFET exhibited no improvements at 20 K compared to room temperature. Therefore it would not be a good device for cryogenic operation. For the measured normally-off GaN HEMT, the on-state resistance improves isotropically from room temperature down to 20 K and exhibits no carrier freeze-out effects. The turn-on voltage of the reverse body diode also reduced with decreasing temperatures which is the opposite of the power MOSFET. This would reduce the voltage drop across the diode. In terms of operating with low power losses at temperatures below 50 K, the GaN HEMT appears to be the most optimised device for the application. However, the current commercially available GaN HEMTs are limited in both current and voltage ratings, therefore their usage in high power applications is restricted.

For the measured Si power Schottky diodes, it was found that they were all operating as MPS diodes at room temperatures. At cryogenic temperatures, the turn-on voltage of the PN junction increase towards 1 V and the Schottky barrier dominates at forward voltages below. The MPS like Schottky diodes exhibited high conductivity at room temperature due to the conductivity modulation of the drift region by bipolar injection from the P+ guard



rings. Therefore, the improvements from higher electron mobility at cryogenic temperatures were nullified when compared to their room temperature behaviour. In this sense, the power Schottky diodes exhibited no improvements at cryogenic temperatures. GaAs Schottky diodes exhibited some power loss improvements at higher current levels but the voltage drop is still limited by the forward turn-on voltage. SiC Schottky diodes exhibited no improvements at cryogenic temperatures, however they have the capability to provide the highest breakdown voltage when compared to other commercially available Schottky diodes.

For the on-state behaviour, a summary of the main findings is shown in Fig. 5.35. The figure compares the observed behaviour for all the measured devices at their known temperature range.

On-state behaviour			
Temperature range	20 K – 50 K		50 K – 100 K
Si n-channel MOSFETs/SJ MOSFETs	<div> <div>Little degradation in the on-state</div> <div>-OR-</div> <div>Non-ohmic behaviour and negative temperature dependence</div> </div>		Optimum range
Si p-channel MOSFETs	<div> <div>Negative temperature dependence</div> <div>Non-ohmic behaviour</div> </div>		Optimum range
SiC MOSFETs	<div> <div>Positive temperature dependence</div> <div>No improvements compared to higher temperatures</div> </div>		Negative temperature dependence
GaN HEMTs	<div> <div>Almost temperature independent</div> <div>Improvements</div> </div>		Small positive temperature dependence
Si/SiC Schottky diodes	No improvements compared to higher temperatures		
GaAs Schottky diodes	Improvements at high current levels		

Figure 5.35: The summarised findings of the on-state behaviour for all the measured devices.

In conclusion, in terms of commercially available power devices, silicon n-channel power MOSFETs are the most optimised for cryogenic applications. They can achieve extremely

low on-state resistance and reasonable breakdown voltages. Therefore, they should be used for the free-wheeling application. A large portion of the measured devices experienced carrier freeze-out effects but a few devices did not. This will be analysed in the next chapter. GaN HEMTs have very good potential in cryogenic applications but are still an immature semiconductor material for high power devices.

# Analysis of the Power MOSFET Cryogenic Behaviour

Power MOSFETs are more optimised than other commercially available power devices to achieve ultra-low on-state resistance at cryogenic temperatures. However, the previous chapter has shown that they can also exhibit some undesirable behaviour, such as carrier freeze-out and breakdown voltage degradation. Furthermore, all the measured reverse body diodes show no improvements at cryogenic temperatures. However, this can be overcome by synchronous rectification and therefore can be overlooked [104]. In this chapter, characteristics such as on-state behaviour and breakdown voltage degradation will be analysed and interpreted through known theory.

The author would like to note that although several attempts have been made to simulate the cryogenic behaviour of power devices with simulators such as Synopsys's Taurus Medici and Silvaco's ATLAS, it is known that they have a quadratic convergence problem when simulating device behaviour at temperatures below 50 K [105]. This is mainly due to parameters such as intrinsic carrier concentration reaching infinitesimal values at cryogenic temperatures, which goes beyond the calculating range of the computation available. Therefore, their function in the analysis of cryogenic behaviour of power devices are limited without a thorough alteration in the physical models used in those simulators.

## 6.1 On-state Resistance Contribution

The total on-state resistance ( $R_{ON}$ ) of a power MOSFET is the sum of several different resistances:

$$R_{ON} = R_{chan} + R_{accu} + R_{JFET} + R_{drift} + R_s. \quad (6.1)$$

All variables have previously been stated in Chapter 2. The percentage contribution of each parameter depends on the voltage rating of the power MOSFET. From Baliga's analysis of a 50 V n-channel VDMOS device,  $R_{JFET} + R_{drift}$  contribute towards  $\sim 24\%$  of  $R_{ON}$ ,  $R_{chan} + R_{accum}$  is 71% of  $R_{ON}$  and  $R_s$  is  $\sim 5\%$  [23]. However, these relative proportions change with temperature and, above 50 K, the changes are mainly due to the temperature dependence of electron mobility. In order to understand the temperature dependent contribution of each resistance parameter, each will be calculated for a 500 V and a 100 V VDMOS.  $R_s$  will be ignored in this analysis since it becomes negligible for higher rated voltage devices and it also depends on the individual type of device packaging. The electron mobility for the drift region and the JFET region can be approximated by the Klasseen equations presented in Chapter 3.2 and the inversion layer and accumulation layer electron mobility can be approximated by equations discussed in Chapter 3.2.

Assuming the gate structure of a 500 V and a 100 V VDMOS device are identical, the main differences between the two will be the dopant concentration of the drift region ( $N_{drift}$ ) and the drift region thickness ( $W_t$ ). Both values can be approximated by the following equations [23]:

$$N_{drift} = -^{3/4}\sqrt{\frac{V_{BD}}{5.34 \times 10^{13}}}, \quad (6.2)$$

$$W_t = 2.67 \times 10^{10} N_{drift}^{-7/8}. \quad (6.3)$$

For a 500 V device,  $N_{drift}$  would be  $5 \times 10^{14} \text{ cm}^{-3}$  and  $W_t$  would be  $3.67 \times 10^{-3} \text{ cm}$ . For a 100 V device,  $N_{drift}$  would be  $4.3 \times 10^{15} \text{ cm}^{-3}$  and  $W_t$  would be  $5.58 \times 10^{-4} \text{ cm}$ . Equations for each of the specific on-state resistance contributors are presented below from Eqn. 6.4

to 6.10 [23]. All the geometric parameters are illustrated in Fig. 6.1. The oxide thickness is approximated to be  $5 \times 10^{-6} \text{ cm}$  and  $V_{GS} - V_{Gth} \approx 10 \text{ V}$  to ensure the device is fully on. It is also common practice to increase the dopant concentration at the JFET region of the MOSFET in order to improve conductivity and reduce the depletion width in the JFET region itself [104]. Therefore  $N_{JFET}$  is approximated as  $2 \times 10^{16} \text{ cm}^{-3}$ . Other values used in the calculation for Eqn. 6.4 to 6.10 are presented in Table. 6.1.

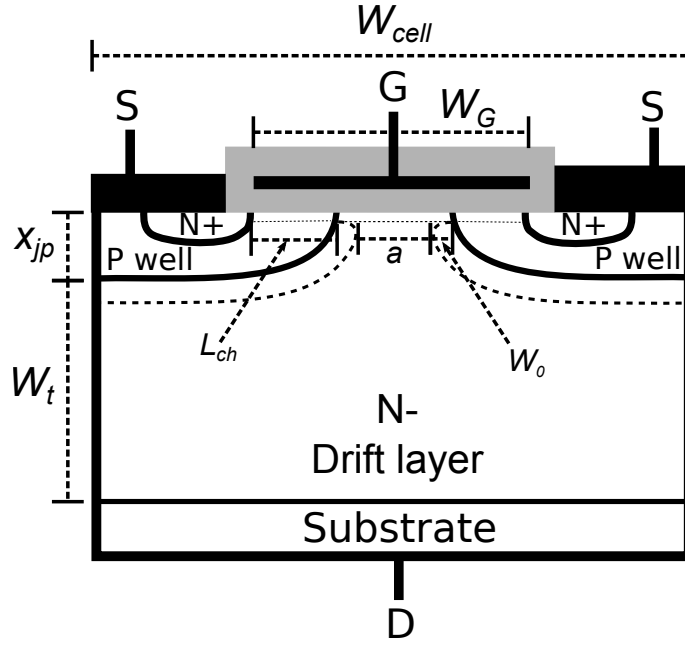


Figure 6.1: Illustration of the geometric parameters used in Eqn. 6.4 to 6.10.

$$R_{drift} = \frac{W_{cell} W_t}{q \mu_n(T, N_{drift}) N_{drift} (W_{cell} - a)} \ln \left( \frac{W_{cell}}{a} \right), \quad (6.4)$$

where  $a$  is the approximation of the dynamic width of the JFET region conduction path,

$$a = W_G - 2x_{jp} - 2W_0, \quad (6.5)$$

where  $W_0$  is the depletion width at the JFET region,

$$W_0 = \sqrt{\frac{2\varepsilon_s N_A V_{bi}}{q N_{JFET} (N_A + N_{JFET})}}. \quad (6.6)$$

and  $V_{bi}$  is the built in voltage of the PN junction,

$$V_{bi} = \left( \frac{kT}{q} \right) \ln \left( \frac{N_A N_{JFET}}{n_i} \right), \quad (6.7)$$

$$R_{JFET} = \frac{x_{jp} W_{cell}}{q \mu_n(T, N_{JFET}) N_{JFET} (W_G - 2x_{jp} - 2W_0)}, \quad (6.8)$$

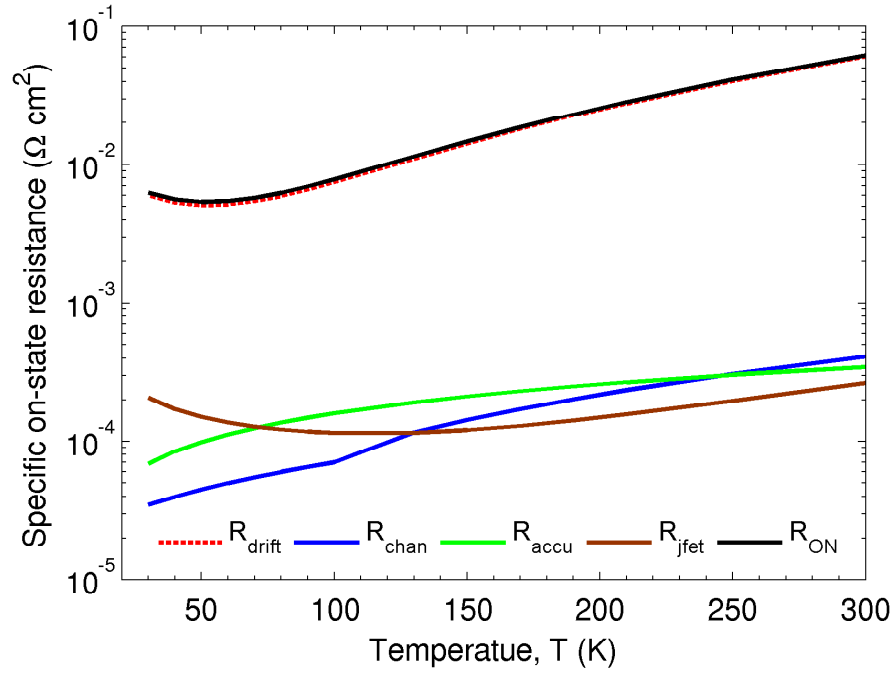
$$R_{chan} = \frac{L_{ch} W_{cell}}{2 \mu_{inv}(T, V_{GS}, N_{chan}) C_{OX} (V_{GS} - V_{Gth})}, \quad (6.9)$$

$$R_{accu} = 0.6 \frac{(W_G - 2x_{jp}) W_{cell}}{4 \mu_{accu}(T, V_{GS} - V_{Gth}, N_{JFET}) C_{OX} (V_{GS} - V_{Gth})}. \quad (6.10)$$

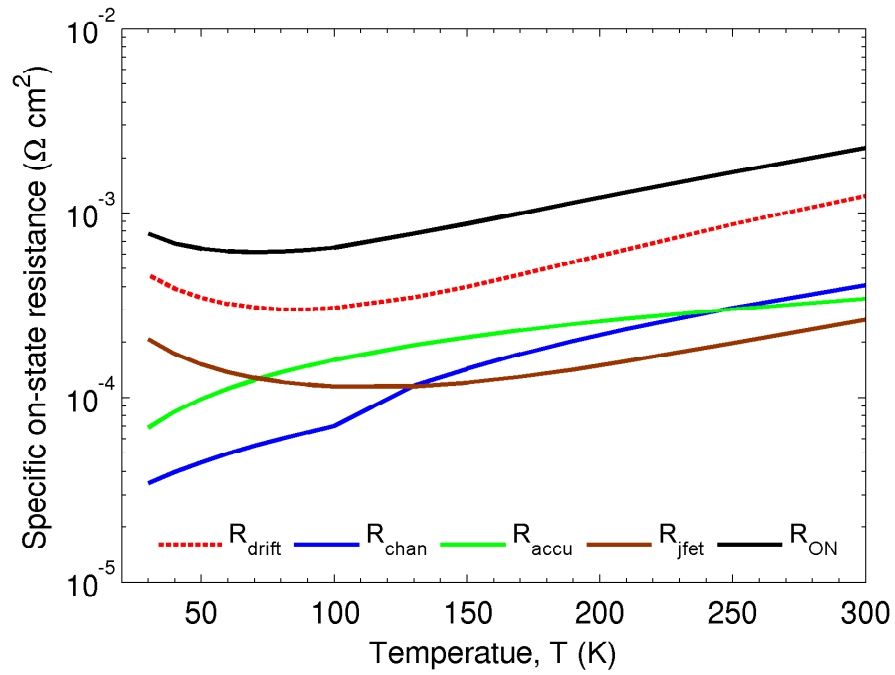
Table 6.1: Values used in Eqn. 6.4 to 6.10.

Parameter	Value
$W_{cell}$	20 $\mu m$
$W_G$	10 $\mu m$
$x_{jp}$	2 $\mu m$
$N_A$	$1 \times 10^{17} \text{ cm}^{-3}$
$L_{ch}$	1 $\mu m$

The calculated temperature dependence of each of the specific on-state resistance contributions are presented in Fig. 6.2 for the 500 V and 100 V devices, including the total specific on-state resistance ( $R_{ON}$ ). For both devices, the drift region on-state resistance dominates at all temperatures, which shows the significance of  $R_{drift}$  contribution. For the 500 V device,  $R_{ON} \approx R_{drift}$ . However, for the three remaining contributions,  $R_{JFET}$  appears to be dominant at temperatures below  $\sim 70$  K. For the 100 V device, because of the lower overall on-state resistance,  $R_{JFET}$  contributes much more towards  $R_{ON}$  even though the dominant contribution is still  $R_{drift}$ .



(a) 500 V device



(b) 100 V device

Figure 6.2: The calculated temperature dependence of the specific on-state resistance due to change in electron mobility of (a) 500 V and (b) 100 V VDMOS devices and the four main contributions.

## 6.2 Modelling the Free Carrier Concentration

In the previous analysis of 6.1, the calculations only took into account the temperature dependence of the electron mobility in the various regions. This analysis can only explain some of the behaviour of the measured MOSFETs. Mainly, the decrease in the on-state resistance above 50 K. At temperatures below 50 K, some devices exhibited a large increase in on-state resistance. This means other factors must contribute towards  $R_{ON}$ . The most well known factor is the carrier freeze-out effect which has previously been discussed in Chapter 3.2.

The carrier freeze-out effect is dependent on temperature but as presented in Chapter 3.2, it is also dependent on the dopant concentration of the silicon. Using the empirical model by Schenk et al. [73], the temperature and dopant concentration dependence of the incomplete ionisation of phosphorus in silicon is presented in Fig. 6.3. It shows that although incomplete ionisation occurs at room temperature it only has a serious impact at high dopant concentrations, (above  $1 \times 10^{16} \text{ cm}^{-3}$ ) and is worst at dopant concentrations around  $1 \times 10^{18} \text{ cm}^{-3}$ . The ionisation proportion increases at higher dopant concentrations due to the merging of the donor energy band and the conduction band. This is when silicon becomes degenerate and ionisation of dopants are no longer required.

Fig. 6.3 shows that at lower temperatures the proportion of ionised dopants reduces. Below 100 K even lower doped silicon is affected and at 20 K the model predicts that virtually no dopants will be ionised for conduction, even with  $N_D$  as low as  $1 \times 10^{13} \text{ cm}^{-3}$ . This is because the thermal energy,  $kT$  from Eqn. 3.10, becomes smaller than the energy required to thermally excite the electrons from the dopant sites to the conduction band. Therefore, if thermal excitation is the only ionisation process then electrical conduction would simply not be possible at 20 K. However, from the measured data in Chapter 5, we know that this is not the case, as at 20 K all power MOSFETs were still able to conduct. This means that there must be one or more additional effects that contribute towards dopant ionisation.

One of the most likely ionisation effects is the Poole-Frenkel ionisation, previously discussed in Chapter 3.2. By combining the Poole-Frenkel ionisation and the incomplete ionisation model by Schenk et al. where the ionisation energy  $E_i$  becomes dependent on the



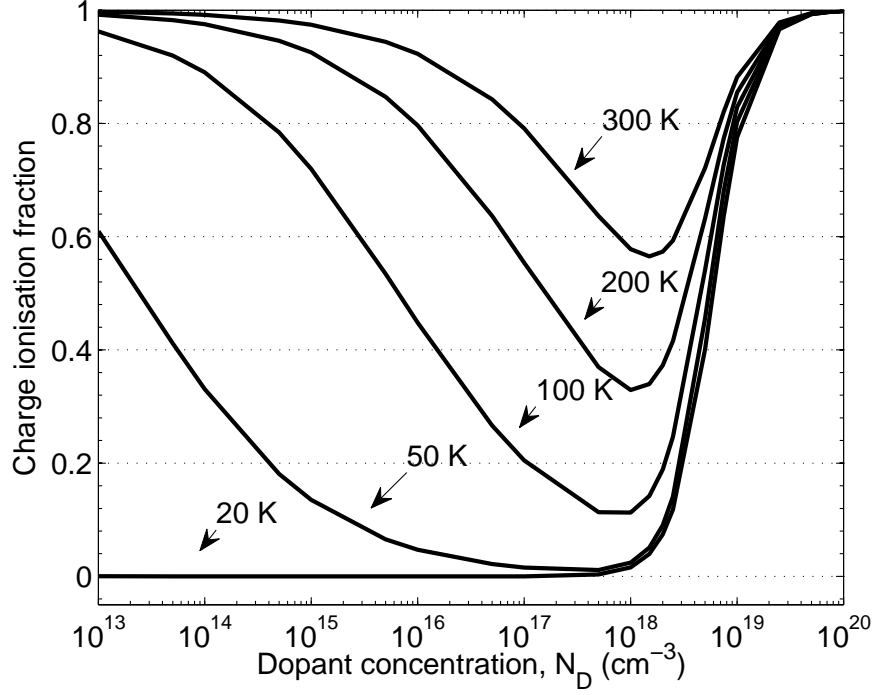


Figure 6.3: The calculated charge ionisation fraction of phosphorus in silicon at different dopant concentration and temperatures.

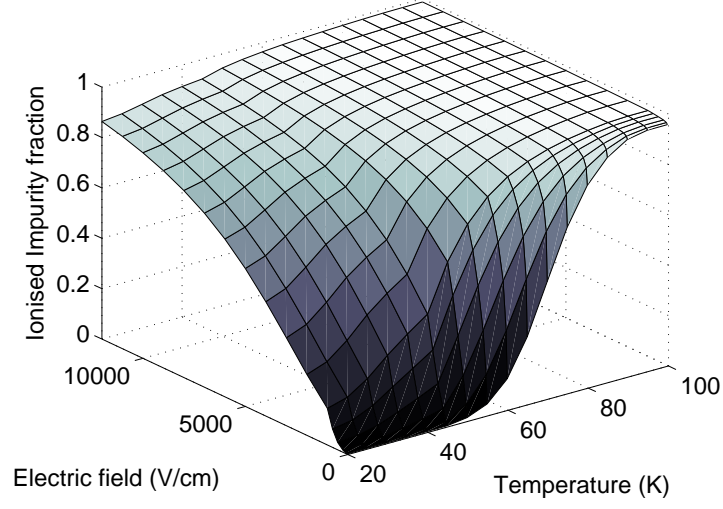
electric field and Eqn. 3.11 becomes Eqn. 6.11, it is possible to predict the ionised dopant concentration in terms of both electric field and temperature.

$$E_{dop} = \frac{E'_i(\mathbb{E})}{1 + (N_D/N_{ref})^C}, \quad (6.11)$$

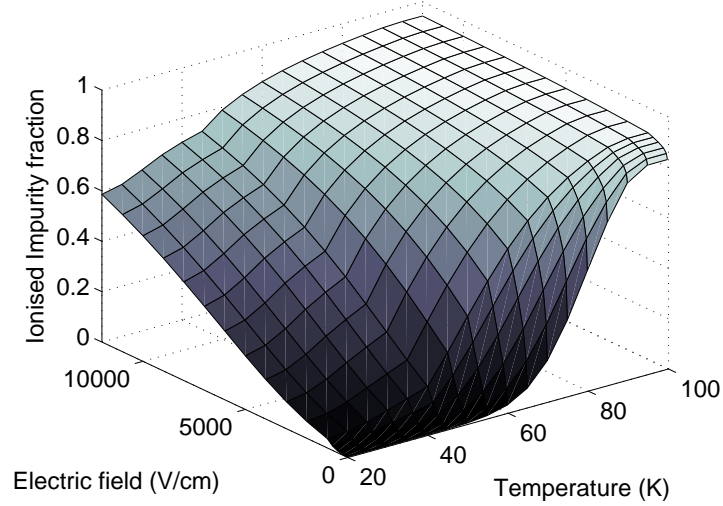
Fig. 6.4 presents the calculated charge ionisation fraction for  $N_D = 5 \times 10^{14} \text{ cm}^{-3}$  and  $1 \times 10^{16} \text{ cm}^{-3}$  at different temperatures and electric field conditions during on-state.

In Fig. 6.4(a), the model predicts that at sufficient electric field conditions a relatively high proportion of the dopant concentration can be ionised for conduction. However, with higher dopant concentration in Fig. 6.4(b), a higher electric field would be required to ionise the same proportion of dopants. However, it is important to bear in mind at  $\mathbb{E} = 12000 \text{ V/cm}$ , 60% of  $1 \times 10^{16} \text{ cm}^{-3}$  is still higher than 85% of  $5 \times 10^{14} \text{ cm}^{-3}$ .

Fig. 6.5 compares the calculated charge ionisation fraction with different dopant concentrations and electric fields at 20 K and 100 K. It is clear that at 100 K, only the narrow



(a)  $N_D = 5 \times 10^{14} \text{ cm}^{-3}$



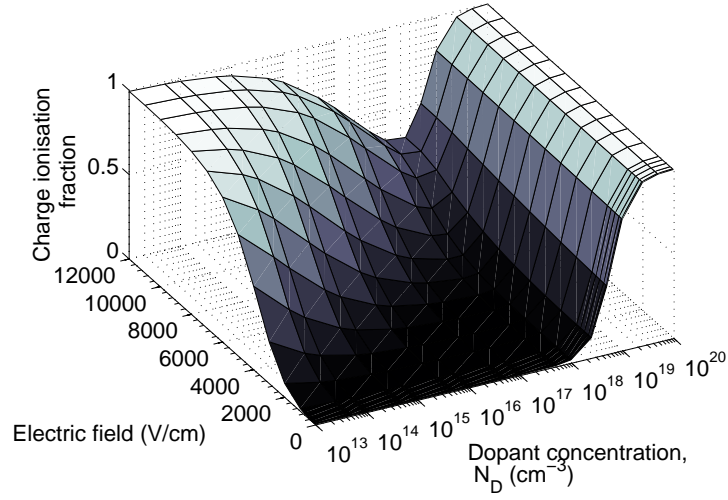
(b)  $N_D = 1 \times 10^{16} \text{ cm}^{-3}$

Figure 6.4: The charge ionisation fraction at different temperatures and electric field conditions for silicon with  $N_D =$  (a)  $5 \times 10^{14} \text{ cm}^{-3}$  and (b)  $1 \times 10^{16} \text{ cm}^{-3}$  during on-state.

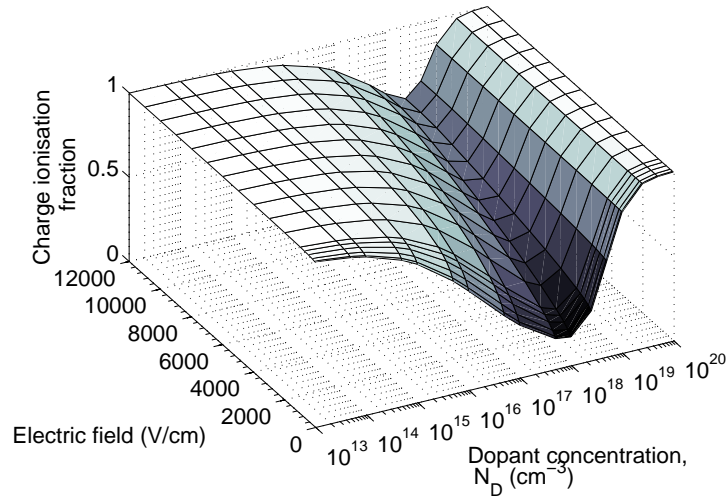
band of  $N_D$  around  $1 \times 10^{18} \text{ cm}^{-3}$  is affected by incomplete ionisation. At 20 K, complete ionisation is only possible at very high dopant concentrations and sufficiently high electric field strengths. This means that for power MOSFETs with high voltage ratings (which commonly have lower dopant concentration in the drift region), a relatively large proportion of the dopant concentration is ionised. However, for lower voltage rated power MOSFETs

## 6.2 Modelling the Free Carrier Concentration

(which commonly have higher dopant concentration in the drift region), a lower proportion of the dopant concentration is ionised and incomplete ionisation is more severe for the same electric field strength.



(a)  $T = 20$  K



(b)  $T = 100$  K

Figure 6.5: The charge ionisation fraction at different dopant concentration and electric field conditions for  $T =$  (a) 20 K and (a) 100 K.

### 6.3 Electric Field and Temperature Dependence of $R_{drift}$ and $R_{JFET}$

At carrier freeze-out temperatures ( $< 50$  K), when  $V_{GS} > V_{Gth}$ , carrier freeze-out effects can be considered negligible for the channel and accumulation layers since they experience sufficient electric field at the oxide interface. Therefore in this section, we can consider the free carrier concentration in those layers is predominately driven by the gate voltage and not by temperature. Therefore only the temperature and electric field effects on  $R_{drift}$  and  $R_{JFET}$  will be analysed in this section at carrier freeze-out temperatures.

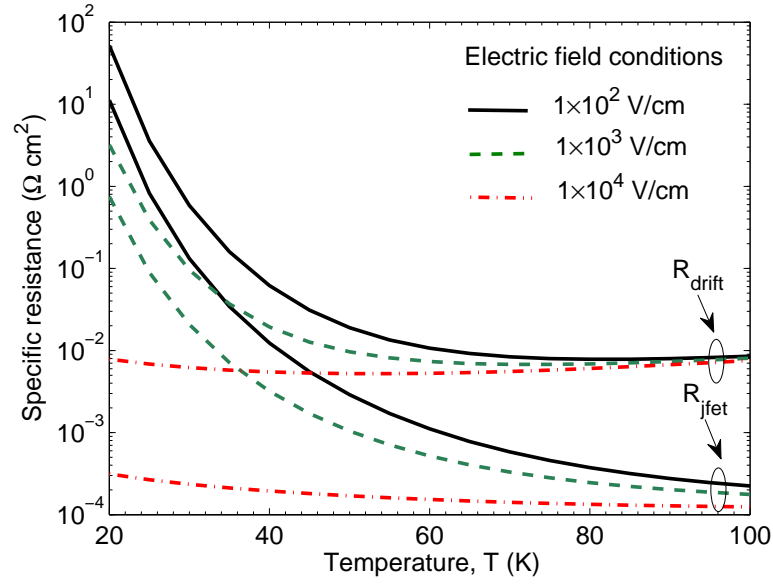
To understand the significance of the electric field dependent carrier freeze-out effects, the temperature, dopant concentration and electric field dependent free carrier concentration ( $n$ ) can be combined with the equations in Chapter 6.1. Hence equations 6.4 and 6.8 become:

$$R_{drift} = \frac{W_{cell}W_t}{q\mu_n(T, N_{drift})n(T, N_{drift}, \mathbb{E})(W_{cell} - a)} \ln \left( \frac{W_{cell}}{a} \right). \quad (6.12)$$

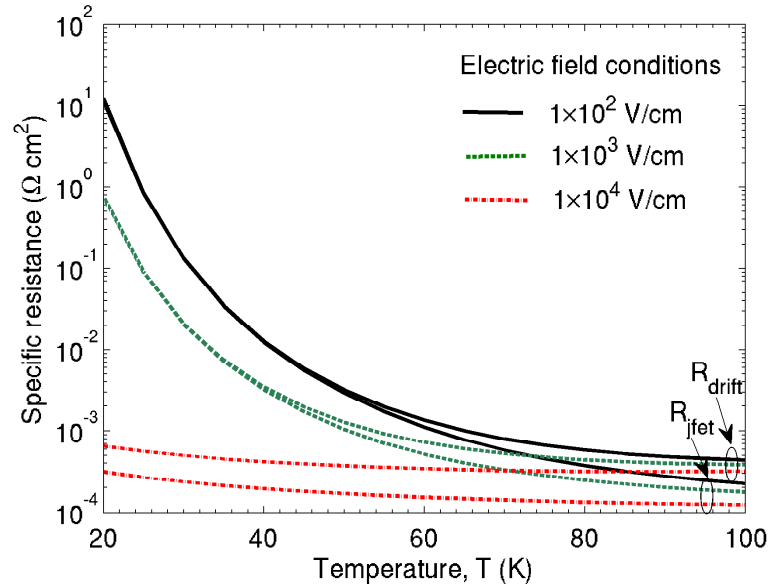
$$R_{JFET} = \frac{x_{jp}W_{cell}}{q\mu_n(T, N_{JFET})n(T, N_{JFET}, \mathbb{E})(W_G - 2x_{jp} - 2W_0)}, \quad (6.13)$$

The electric field dependence of the specific resistance of  $R_{drift}$  and  $R_{JFET}$  at carrier freeze-out temperatures can now be calculated. Fig. 6.6 presents  $R_{drift}$  and  $R_{JFET}$  at different electric field and temperature conditions for 500 V and 100 V VDMOS structures. Fig. 6.6(a) shows that at 100 K  $R_{drift}$  is generally independent of the electric field strength. However, as temperature decreases  $R_{drift}$  becomes increasingly dependent on the electric field. At  $\mathbb{E} \leq 1 \times 10^3$  V/cm the specific resistance increases quite dramatically. At  $\mathbb{E} \geq 1 \times 10^4$  V/cm  $R_{drift}$  remains relatively low even temperatures below 50 K. The data shows that  $R_{JFET}$  is electric field dependent at 100 K. Furthermore, at  $\mathbb{E} \leq 1 \times 10^3$  V/cm  $R_{JFET}$  becomes comparable to  $R_{drift}$  at temperatures below 50 K. Fig. 6.6(b) shows that both  $R_{drift}$  and  $R_{JFET}$  are electric field dependent at 100 K. Interestingly, at  $\mathbb{E} \leq 1 \times 10^3$  V/cm and assuming both the drift and JFET region experience the same electric field, their specific resistance becomes almost identical at temperatures below 50 K.

### 6.3 Electric Field and Temperature Dependence of $R_{drift}$ and $R_{JFET}$



(a) 500 V device



(b) 100 V device

Figure 6.6: The calculated temperature dependent specific on-state resistance of the drift region ( $R_{drift}$ ) and JFET region ( $R_{JFET}$ ) for a (a) 500 V and a (b) 100 V VDMOS at different electric field conditions.

In normal operating conditions, if the dopant concentration at the JFET region is the same as the drift region the electric field across the two can be assumed to be the same.

However, since most VDMOS devices have a higher doped JFET region, and therefore lower resistance and reduced voltage drop, the electric field within the JFET region would be lower than the drift region. Fig. 6.7 shows the two dimensional electric field profile of a 200 V VDMOS at room temperature during conduction simulated using MEDICI. When the dopant concentration profile of the JFET region is not accurately controlled,  $R_{JFET}$  can contribute in various degrees towards  $R_{ON}$ . This shows that although  $R_{JFET}$  is a relatively minor contributor towards  $R_{ON}$  at normal operating temperatures, at carrier freeze-out temperatures and low electric field conditions, it could become a major contributor.

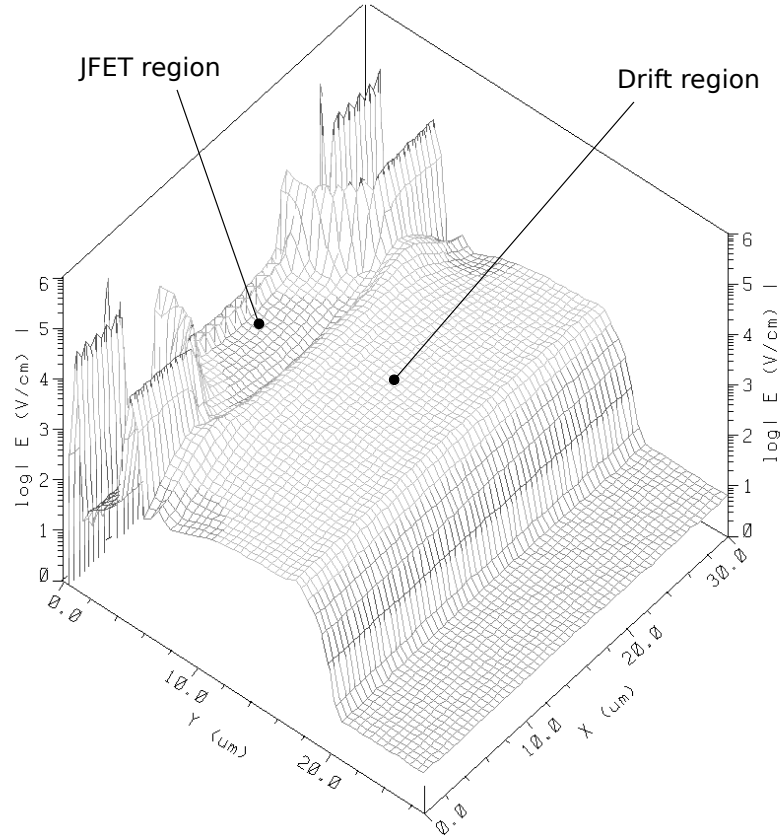


Figure 6.7: Electric field profile of a 200 V VDMOS at room temperature indicating the lower electric field experienced in the JFET region due to higher dopant concentration simulated using MEDICI.

## 6.4 Comparison of Calculated and Measured Data

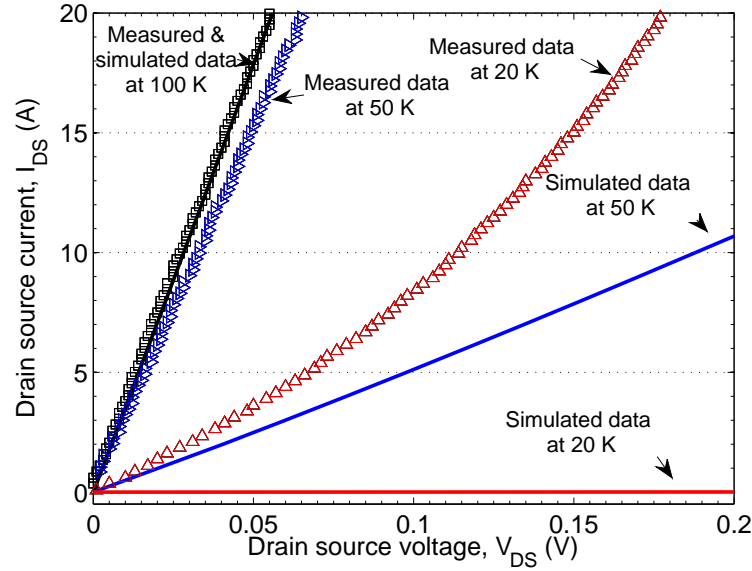
Assuming drift and JFET region are the only contributors toward  $R_{ON}$ , and accounting for the temperature dependent electron mobility, carrier freeze-out and the electric field dependent ionisation, the IV characteristics of a 200 V and a 500 V were modelled using previously introduced equations and compared with the data presented in Fig. 6.8 at the temperature of 100 K, 50 K and 20 K.

Although an exact match was not expected, the correlation between the measured and calculated behaviour was found to be poor at 50 K and 20 K. The calculation predicted that at 20 K, the device would not be operational at the calculated voltage range. At 50 K, the calculation predicted the device would have a much higher on-state resistance than suggested by the measured data. This is mainly due to the modelling of the low electric field across the drift and JFET region, which is not high enough to ionise sufficient charge carriers for a good conduction. However, the measured data suggested that even at virtually zero applied voltage (no electric field across the drift region) there is an adequate amount of free charge carriers in the drift and JFET regions for good conduction. This was not predicted from the previously discussed model.

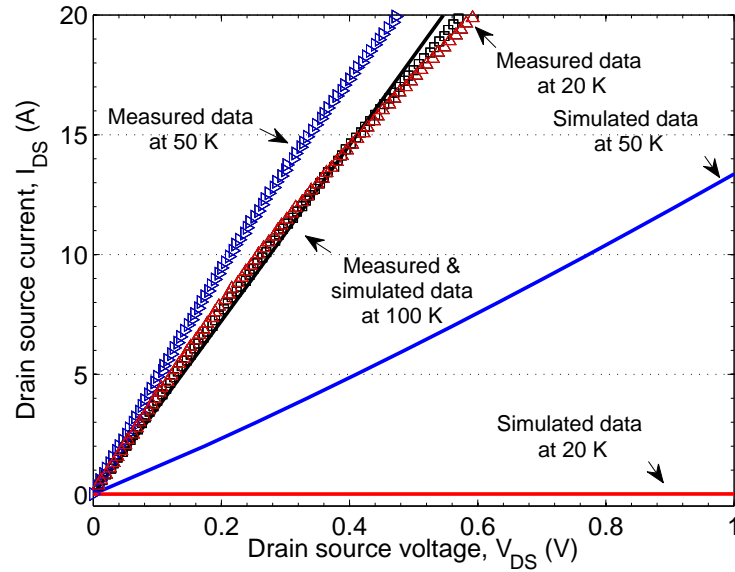
In order to assess the free carrier concentration of the two measured devices, the initial (zero volts)  $n$  of the drift and JFET regions were modified to match the measured data (see Eqn. 3.8 to 3.11 and Eqn. 6.11). The results are shown in Fig. 6.9(a) and 6.9(c). In addition, Fig. 6.9(b) and 6.9(d) presents the modified carrier concentration which changes with voltage across the drift region. In Fig. 6.9(a), with the increased initial free carrier concentration, the calculated data matches reasonably well with measured data. The non-ohmic behaviour due to the Poole-Frenkel ionisation in the drift and JFET region can also be seen in the calculation where dopant ionisation increases with higher voltages. Fig. 6.9(c) did not show any non-ohmic behaviour since the initial free carrier concentration was fairly close to the dopant concentration of the drift region. The changes with voltage due to the Poole-Frenkel ionisation were too low to be noticeable in the IV characteristics.

With the aim of achieving ultra-low power loss with power MOSFETs, the low voltage on-state resistance is crucial. The above analysis shows the importance of the initial free

## 6.4 Comparison of Calculated and Measured Data



(a) 200 V device



(b) 500 V device

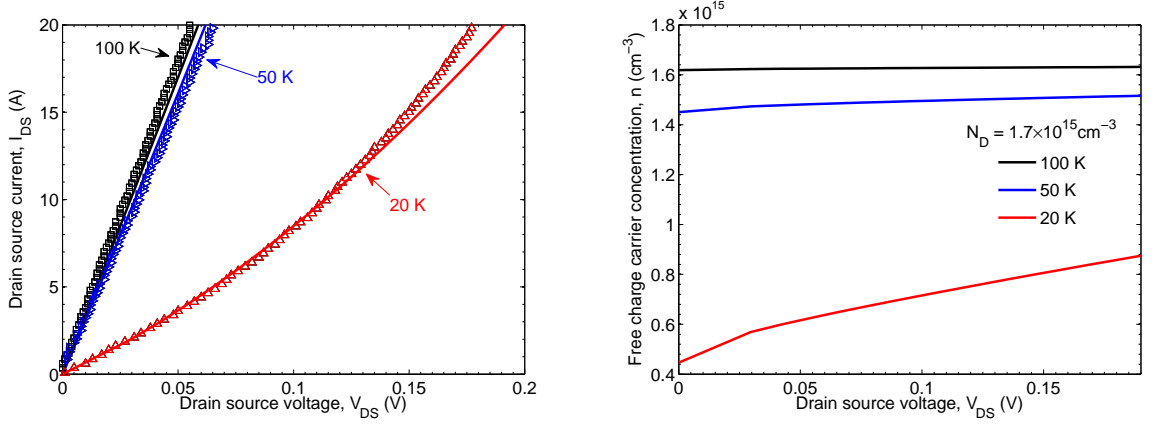
Figure 6.8: Comparison between the calculated IV characteristics of the sum of the drift and JFET region of a 200 V and a 500 V device and measured data of the 200 V and 500 V HEXFET presented in Fig. 5.2(c) and 5.18(a).

carrier concentration parameter, since this dictates the low voltage on-state resistance of the power MOSFET in the carrier freeze-out temperature range. By using the adjusted initial

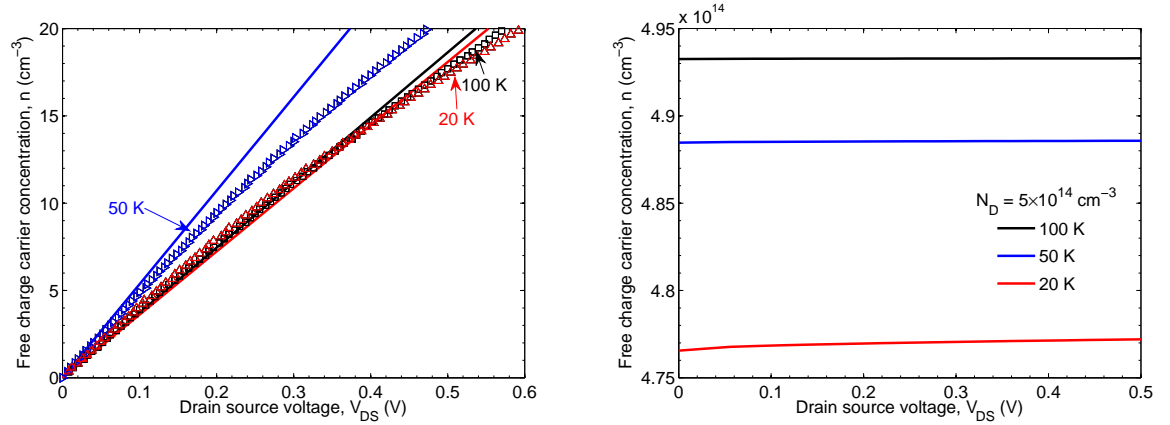


## 6.4 Comparison of Calculated and Measured Data

free carrier concentration, the calculation produced similar behaviour when compared to the measured data. However, this raises another question: *Where did the initial free carrier concentration come from?* At 20 K, the model suggested that the drift and JFET region at any dopant concentration would be completely frozen-out; yet the measured data suggested otherwise. Furthermore, the initial free carrier concentration can be different even between supposedly identical devices, as shown in the previous chapter.



(a) Matched IV characteristics for the 200 V device (b) Calculated free carrier concentration at the drift region with voltages



(c) Matched IV characteristics for the 500 V device (d) Calculated free carrier concentration at the drift region with voltages

Figure 6.9: Matching the calculated data with the measured data of the 200 V and 500 V device with increased initial free carrier concentration, (a) the matched IV characteristics for the 200 V device, (b) the calculated free carrier concentration at the drift region for the 200 V device, (c) the matched IV characteristics for the 500 V device and (d) the calculated free carrier concentration at the drift region for the 200 V device.

## 6.5 Initial Free Carrier Concentration

An interpretation of this behaviour is that when  $V_{GS} \gg V_{Gth}$ , accumulation layers are formed due to the field effect under the gate oxide at the throat of the JFET region. When a voltage is then applied across drain and source, electrons can be injected from the accumulation layer into the frozen charge carrier regions via a process similar to space charge limited conduction (see Fig. 6.10). Ignoring any trapping effects, the initial current through the two regions would follow the Mott-Gurney Law [61]:

$$I = \frac{9a\varepsilon_{si}\varepsilon_0\mu_n(T, N_D)(V_{drift} + V_{JFET})^2}{8(W + (x_{jp} - x_{accu}))^3}, \quad (6.14)$$

where  $V_{drift}$  and  $V_{JFET}$  are the voltages across the drift and JFET regions respectively and  $x_{accu}$  is the thickness of the accumulation layer. Following the derivation in [106],  $x_{accu}$  can be approximated as:

$$x_{accu} = \sqrt{2}L_D \cos^{-1} \left( \exp \left( \frac{q\phi_S}{2kT} \right) \right), \quad (6.15)$$

where  $L_D$  is the Debye length, given as:

$$L_D = \sqrt{\frac{\varepsilon_{si}\varepsilon_0kT}{q^2N_D}}, \quad (6.16)$$

and  $\phi_S$  is the surface potential at the oxide and silicon interface. Unlike at room temperatures, where conduction would be instant, at 20 K the electrons injected into the JFET and drift regions would require a certain amount of time to travel across the frozen-out region before reaching the fully ionised highly doped substrate. Injecting electrons into the drift region dramatically improves its conductivity. As seen from the measurements and calculation, with increasing electric field in the drift region, frozen electrons can be ionised via the Poole-Frenkel ionisation process and further increase the free carrier concentration in the drift region.

The space charge limited current through the frozen JFET and drift regions would depend on the source of the current and in this case, the electron concentration of the accumulation

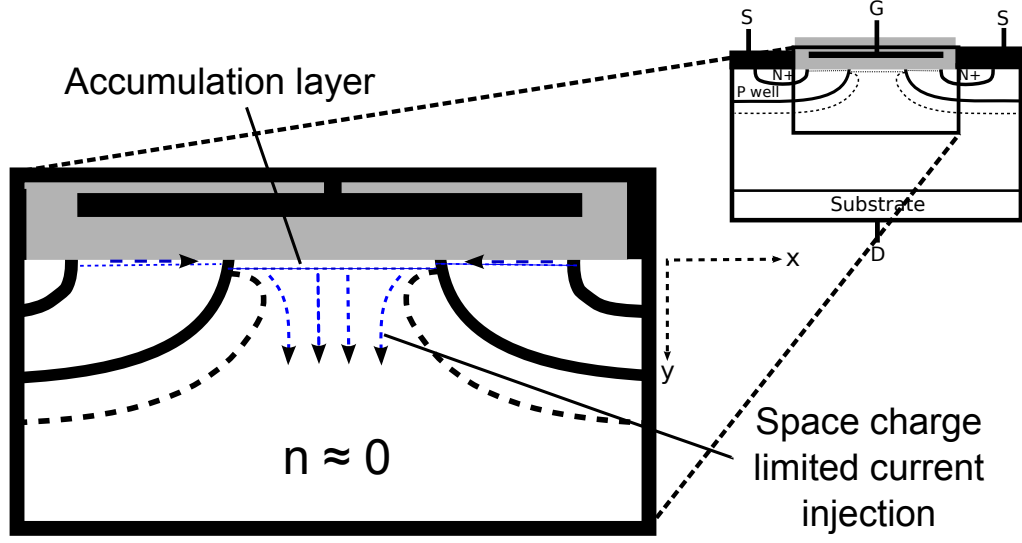


Figure 6.10: A magnified view of the JFET throat region showing the injection of the space charge limited current into the frozen JFET and drift region at carrier freeze-out temperatures.

layers formed from the applied gate voltage. This can be calculated by the following equation [61]:

$$n_{(y)} = N_D \exp \left( -\frac{q\phi_{(y)}}{kT} \right), \quad (6.17)$$

where the free electron concentration ( $n$ ) varies with distance  $y$  from the oxide interface is dependent on the dopant concentration ( $N_D$ ), the potential ( $\phi$ ) with distance  $y$  from the oxide interface and temperature.  $\phi_{(y)}$  can be modelled as:

$$\phi_{(y)} = -\frac{kT}{q} \ln \left( \sec^2 \left[ \cos^{-1} \left( \exp \frac{q\phi_S}{2kT} \right) - \frac{y}{\sqrt{2}L_D} \right] \right), \quad (6.18)$$

The derivation can be found in [106]. The potential along the direction of  $y$  is also dependent on the dopant concentration through  $L_D$ , temperature and the surface potential ( $\phi_S$ ).  $\phi_S$  has the following relationship with the gate voltage ( $V_{GS}$ ):

$$V_{GS} = \phi_S - \frac{\varepsilon_{si}\varepsilon_0\sqrt{2}kT}{C_{OX}L_Dq} \sqrt{\exp \left( -\frac{q\phi_S}{kT} \right) - 1}. \quad (6.19)$$

The calculated  $\phi_{(y)}$  and  $n_{(y)}$  for two different dopant concentrations (for a 200 V and

a 500 V rated drift region) at three different cryogenic temperatures are presented in Fig. 6.11. The calculation assumes  $V_{GS} = 15$  V. Fig. 6.11(a) shows the potential from  $y = 0$  to  $0.1 \mu\text{m}$  and Fig. 6.11(b) shows the free carrier concentration ( $n$ ) over the same distance. The figure shows that the electron concentration in the accumulation layer is much higher than the background dopant concentration and reduces with  $y$  until it drops to the same level. The distance between  $y = 0$  and the point in which  $n = N_D$  is  $x_{accu}$ , which can be calculated from Eqn. 6.15. Both  $\phi_{(y)}$  and  $n_{(y)}$  reduce with decreasing temperatures, however the above equations are only valid above carrier freeze-out temperatures, since they do not take into account any incomplete ionisation effects. Therefore, the calculated 20 K data does not represent the actual behaviour.

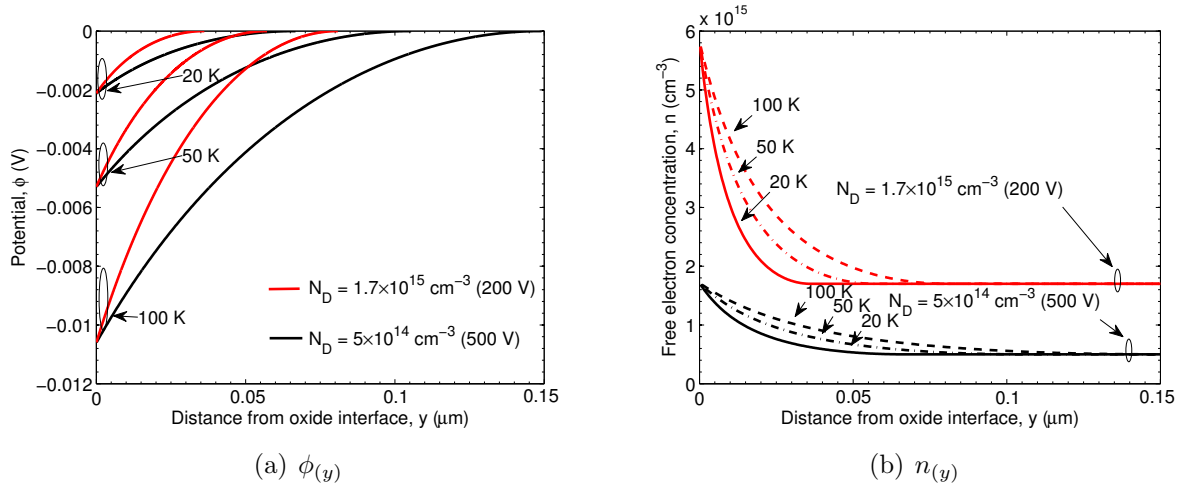


Figure 6.11: The calculated (a) potential,  $\phi_{(y)}$  and (b) free electron concentration,  $n_{(y)}$  against distance from the oxide interface,  $y$  at different dopant concentration and temperatures.

In order to calculate the actual behaviour at carrier freeze-out temperatures, the incomplete ionisation effects and electric field dependence must be integrated into Eqn. 6.17 to become:

$$n_{(y)} = n'_{(y)}(\mathbb{E}_{(y)}, N_D, T) \exp -\frac{q\phi_{(y)}}{kT}, \quad (6.20)$$

where the  $N_D$  becomes the new free carrier concentration ( $n'_{(y)}$ ) which is dependent on the

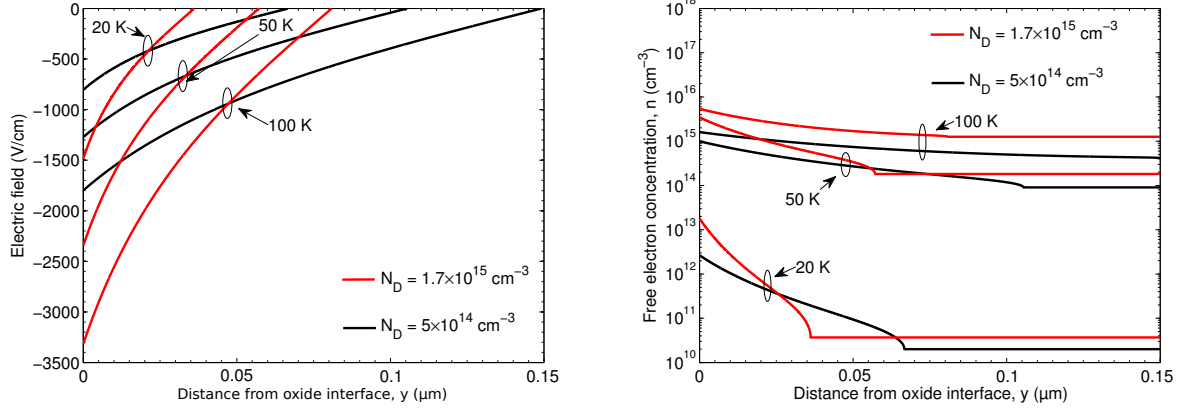
electric field with  $y$ , the background dopant concentration and temperature. This can be calculated using the Poole-Frenkel ionisation effect with the incomplete ionisation models by Schenk et al. in Chapter 3.2. The electric field with  $y$ ,  $\mathbb{E}_{(y)}$ , can be approximated using [106]:

$$\mathbb{E}_{(y)} = \frac{\sqrt{2}KT}{qL_D} \sqrt{\exp\left(-\frac{q\phi_{(y)}}{kT}\right) - 1}. \quad (6.21)$$

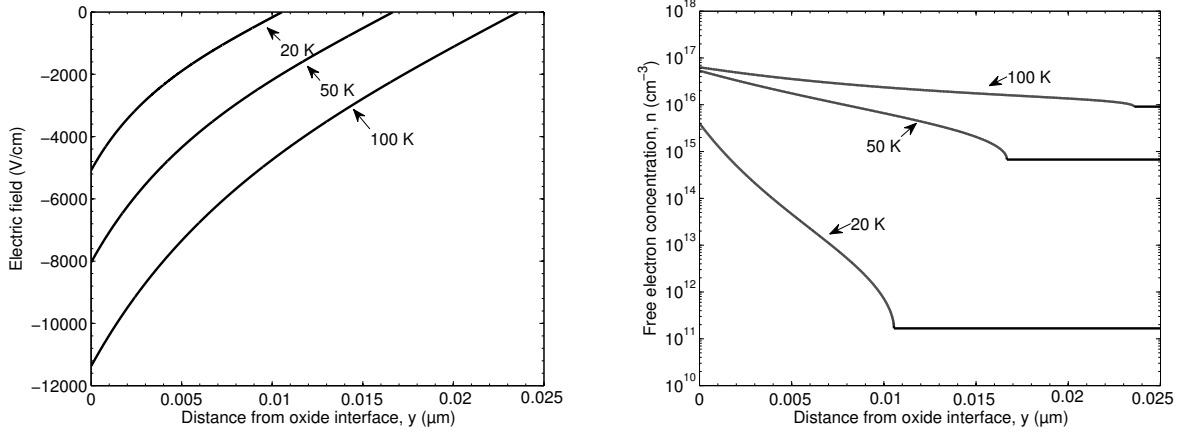
Assuming  $V_{GS} = 15$  V and  $V_{DS} = 0$  V, the calculated changes in electric field with  $y$  are presented in Fig. 6.12(a) at different dopant concentrations and temperatures. A higher dopant concentration would lead to a higher electric field at the silicon-oxide interface but also results in a thinner accumulation layer. The electric field and temperature dependent free electron concentration with  $y$  are presented in Fig. 6.12(b). Unlike the calculation shown in Fig. 6.11(b), the free carrier concentration beyond the accumulation layer does not reduce to  $N_D$ , but reduces to the much lower free carrier concentration as presented. This is due to the carrier freeze-out effects at 20 K and 50 K. However, at 20 K, the calculated data shows that if we assume the accumulation layer would inject electrons into the JFET and drift regions when  $V_{DS} > 0$ , then the free carrier concentration in the accumulation layer is even lower than expected when compared to Fig. 6.9(b) and 6.9(d). This would suggest that this interpretation of electron injection would be incorrect. However, considering that the JFET region is generally doped at a much higher dopant concentration in order to reduce the depletion layer thickness of the JFET effect [104], the dopant concentration near the surface of the oxide would be higher. This would result in higher free carrier concentration in the accumulation layer. Assuming the background doping near the surface of the oxide is at  $2 \times 10^{16} \text{ cm}^{-3}$ , the calculated electric field and free carrier concentration against  $y$  is shown in Fig. 6.12(c) and 6.12(d). Notice the accumulation layer thickness is much lower than seen in Fig. 6.12(a). At 20 K, the accumulation layer is approximately  $1 \times 10^{-6} \text{ cm}$  in thickness and the electric field is also much higher in comparison to Fig. 6.12(a). The free carrier concentration level near the oxide interface is high enough to inject the required initial free carrier concentration estimated in Fig. 6.9(b) and 6.9(d).

According to the above analysis, the background doping concentration of the JFET region near the surface of the oxide interface would be critical in controlling the initial

## 6.5 Initial Free Carrier Concentration



(a)  $E_{(y)}$  for background doping at  $5 \times 10^{14} \text{ cm}^{-3}$  and (b)  $n_{(y)}$  for background doping at  $5 \times 10^{14} \text{ cm}^{-3}$  and  $1.7 \times 10^{15} \text{ cm}^{-3}$



(c)  $E_{(y)}$  for background doping at  $2 \times 10^{16} \text{ cm}^{-3}$  (d)  $n_{(y)}$  for background doping at  $2 \times 10^{16} \text{ cm}^{-3}$

Figure 6.12: (a), (c) are the calculated electric field profile at the accumulation layer for different dopant concentrations and (b), (d) are the electric field and temperature dependent free carrier concentration at the accumulation layer for different dopant concentration.

free carrier concentration at carrier freeze-out temperatures. Any differences in the dopant concentration in the JFET region between otherwise identical devices could result in large differences between their initial free carrier concentrations at freeze-out temperatures, as seen in some of the power MOSFETs presented in the previous chapter. For example, the drift and JFET regions for the 1500 V PowerMESH device in Fig. 5.12 would have a much lower dopant concentration in order to sustain the high breakdown voltage. Therefore, the

background doping concentration near the oxide interface would be much lower. This would result in lower initial free carrier concentration at freeze-out temperatures. The figure shows that at 20 K, the device only begins to significantly conduct at  $V_{DS} > 1$  V. This would suggest a very low initial free carrier concentration and a high electric field requirement to ionise sufficient free carriers via Poole-Frenkel ionisation. This highlights the importance of increased dopant concentration in the region immediately under the gate oxide in order to achieve extremely low on-state resistance at carrier freeze-out temperatures. However, there is a limit to the dopant concentration in this region. If the region is too highly doped, it would lead to lower device breakdown voltages.

As shown in Chapter 5.1.4, the 500 V HEXFET has a lower on-state resistance compared to the average CoolMOS. However, CoolMOS 1 did have the lowest on-state resistance out of all the measured devices in the comparative analysis. Therefore, in terms of on-state behaviour, it may be possible to optimise CoolMOS to achieve the lowest on-state resistance even at freeze-out temperatures.

## 6.6 Thermal behaviour

Since commercially available power MOSFETs are not designed for cryogenic operation, some of their measured on-state behaviour (Chapter 5.1) has been shown to differ considerably in the carrier freeze-out temperature range ( $< 50$  K). Even between supposedly identical devices, the variance is large. Furthermore, the on-state resistance can change substantially within a relatively small temperature range. In order to utilise power MOSFETs at temperatures below 50 K, individual device characterisation would be required to filter out the devices that do not exhibit freeze-out behaviour. This would consume significant time and resources. In the absence of a filtering process, differences between devices could have unexpected effects on their thermal behaviour. If a power MOSFET with strong carrier freeze-out behaviour was employed at 20 K, it would generate high power losses which would increase the junction temperature. However, at this temperature range, the on-state resistance has a negative temperature coefficient so the on-state resistance would actually decrease with increasing

temperature. This would create a self-stabilising mechanism, which means that as long as the power loss is not high enough to elevate the device junction temperatures to a region of positive temperature coefficient, the power loss will automatically stabilise. In addition, when compared with room temperatures, the thermal conductivity of silicon (see Chapter 3.4) is at least an order of magnitude higher at cryogenic temperatures. This means the device retains less heat and the changes in device temperature will be lower by comparison.

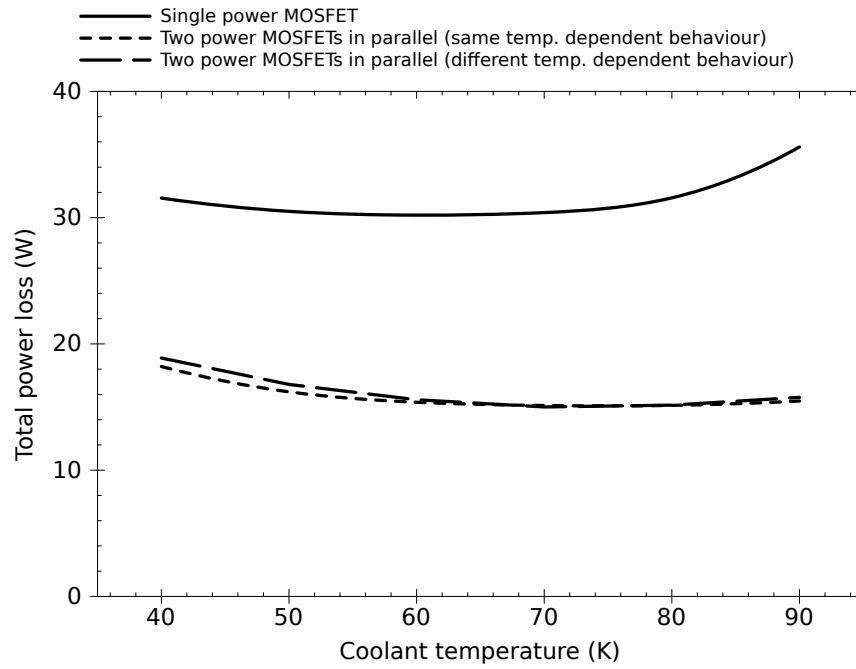


Figure 6.13: Comparison between the calculated temperature dependent steady state power losses for a single 200 V HEXFET, two paralleled 200 V HEXFET with identical temperature dependent on-state resistance and two paralleled 200 V HEXFET with different temperature dependent on-state resistance.

By parallelling power MOSFETs, the temperature dependent steady state power loss can be reduced. If two MOSFETs are paralleled and one of them has a lower on-state resistance, a large proportion of the current will flow through it and in turn elevate the device temperature. This will increase its on-state resistance and reduce its share of the overall current. As the second MOSFET conducts more of the current the temperatures of the two power MOSFETs will eventually stabilise at a similar level. An example of this is shown in Fig. 6.13, where by using the measured temperature dependent on-state resistance,



## 6.7 Temperature Dependent Breakdown Voltages and Effective Ionisation Rates

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the steady state power losses were calculated at 100 A for a single 200 V HEXFET (A1) from Chapter 5.1.1.1, two paralleled A1 and paralleled A1 and A4.

## 6.7 Temperature Dependent Breakdown Voltages and Effective Ionisation Rates

The temperature dependence of the breakdown voltage of power MOSFETs at cryogenic temperatures is an important issue. This is because as temperature decreases the breakdown voltage also decreases from the specified breakdown voltage at room temperature, and this must be taken into account when operating power MOSFETs at cryogenic temperatures. Fig. 6.14 presents the normalised breakdown voltages of various measured power MOSFETs against temperature. The rate of decrease is different for different types of device structure: CoolMOS exhibited the sharpest rate of decrease among the measured devices and MDMesh exhibited the lowest degradation rate. For the two HEXFETs, the difference is relatively small and they follow the dopant concentration dependence trend presented in Fig. 3.18; where a higher dopant concentration should lead to a smaller decrease. However, for the higher doped super-junction (SJ) devices like CoolMOS, this was not the case. This suggests that the structure of the device also plays a role in the temperature dependence of the breakdown voltage. For conventional power MOSFETs such as the HEXFET, although the rate of reduction in breakdown voltage is similar among devices with different blocking voltages, the actual change in breakdown voltage is more significant in higher rated devices. Assuming a 25% drop from room temperature to 20 K, a 500 V device would drop to 375 V whereas a 200 V device would only drop to 150 V.

In order to operate commercially available devices at cryogenic temperatures, the required rated voltage will have to be adjusted for the lowest expected operating temperature of the application. If the lowest expected operating temperature is 20 K and the expected drop is 25%, then in order to get 200 V breakdown, a 270 V device would be required. For 500 V breakdown, a 670 V device would be required. The resulting on-state resistance would also increase accordingly.

## 6.7 Temperature Dependent Breakdown Voltages and Effective Ionisation Rates

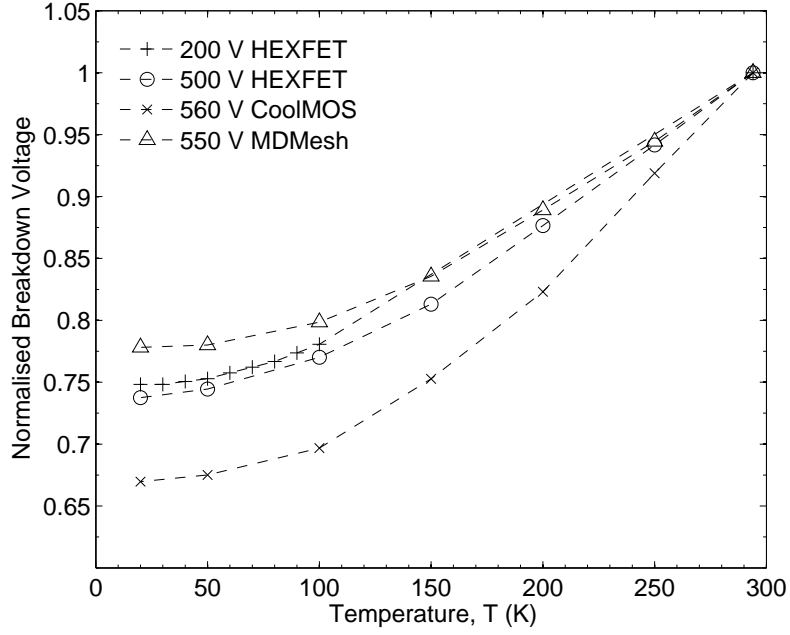


Figure 6.14: Comparison of the normalised temperature dependent breakdown voltages of various power MOSFETs.

From the measured breakdown voltage data, it is clear that the previously assumed linear temperature dependence model proposed by Singh and Baliga from Fig. 3.20(b) is inaccurate. All of the measured data indicates that as  $T$  tends to zero, the ionisation rate saturates towards a lower value than predicted by the linear model. A different model proposed by Okuto and Crowell accounts for saturation of the effective ionisation rate at cryogenic temperatures [107], and it has the following expression:

$$\alpha_{eff} = \left( \frac{q\mathbb{E}}{\xi_i} \right) \exp \left[ 0.217 \left( \frac{E_i}{E_r} \right)^{1.14} - \sqrt{\left( 0.217 \left( \frac{E_i}{E_r} \right)^{1.14} \right)^2 + \left( \frac{E_i}{\mathbb{E}} \right)^2} \right], \quad (6.22)$$

where  $\xi_i$  is the threshold ionisation energy,  $E_i$  is equal to  $\xi_i/(q\lambda)$  and  $E_r$  is equal to  $\xi_r/(q\lambda)$ ,  $\xi_r$  is the optical-photon energy.  $\lambda$  is the mean free path for optical-phonon scattering of energetic carriers. Assuming  $\xi_i = 1.5E_g(T)$ ,  $\xi_r = 0.063 \text{ eV}$  and  $\lambda = 7.6 \times 10^{-7} \text{ cm}$ , and following the above equation, the calculated  $\alpha_{eff}$  against temperature at different electric field strength is presented in Fig. 6.15. The predicted  $\alpha_{eff}$  appears to begin to saturate just

## 6.7 Temperature Dependent Breakdown Voltages and Effective Ionisation Rates

below 150 K and reaches a plateau below 100 K.

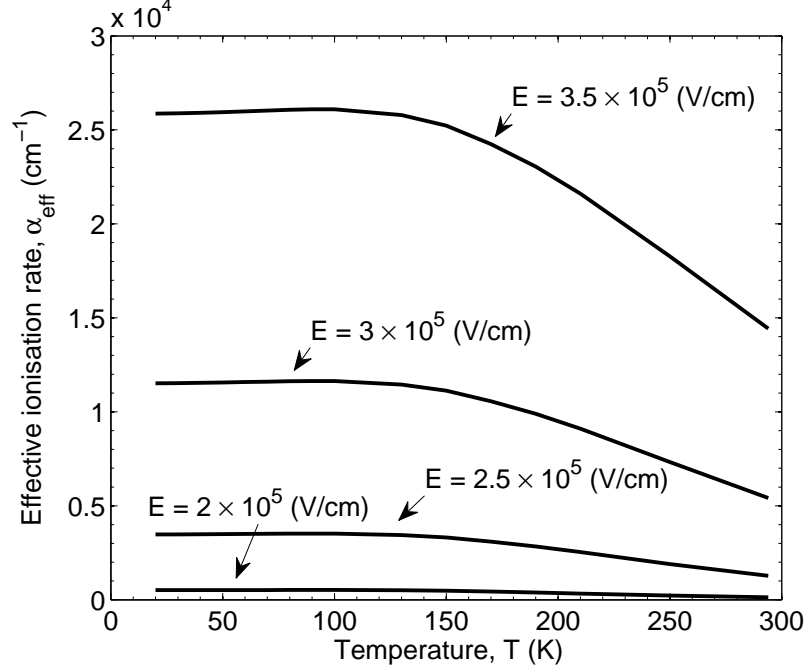


Figure 6.15: The calculated  $\alpha_{eff}$  against temperature at different electric field strength with Eqn. 6.22.

Under the condition of Eqn. 3.28, the calculated breakdown voltages of the different models are compared with measured data for the 500 V HEXFET in Fig. 6.16(a) and for the 200 V HEXFET in 6.16(b). The data shows that the linear model by Singh and Baliga over-estimates the breakdown voltages over a large portion of the temperature range and under-estimates below  $\sim 50$  K. For the Okuto and Crowell model, it over estimates the breakdown voltages below 150 K due to the predicted saturation of  $\alpha_{eff}$ . For conventional power MOSFETs, an empirical equation extracted from the HEXFET measurements has also been added in both figures. This equation can be used to estimate the approximate reduction in breakdown voltage at temperatures below 300 K and is expressed as:

$$V_{BD}(T) = V_{BD}(300)(2.45 \times 10^{-6}T^2 + 2.2 \times 10^{-4}T + 0.729), \quad (6.23)$$

where  $V_{BD}(T)$  is the temperature dependent breakdown voltage and  $V_{BD}(300)$  is the break-

## 6.7 Temperature Dependent Breakdown Voltages and Effective Ionisation Rates

down voltage at 300 K. It should be noted that the actual breakdown voltage of the device at 300 K is generally slightly higher than the specified breakdown voltage and an actual measured  $V_{BD}(300)$  would be more accurate. This approximation does not account for the small temperature dependent differences with different dopant concentrations.

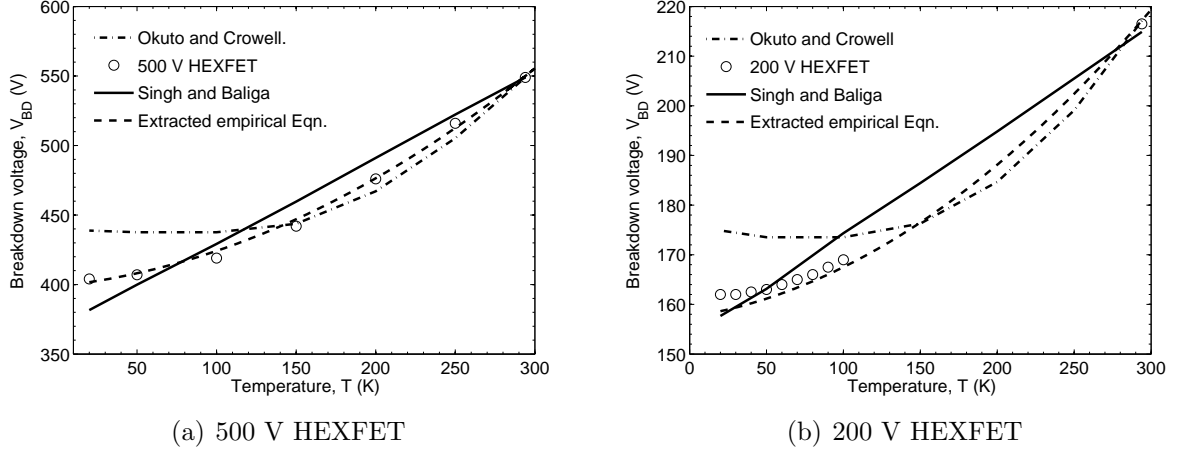


Figure 6.16: Comparison between predicted breakdown voltage with measured data for (a) 500 V HEXFET and (b) 200 V HEXFET.

As seen from Fig. 6.16, all the previous effective ionisation rate models are shown to be inadequate in predicting the actual breakdown voltage. This could be due to a number of reasons. For example, the simplified one dimensional electric field model compared to the actual three dimensional electric field profile of an MOSFET or the unexplored ionisation behaviour at cryogenic temperatures. In order to produce a more accurate model, the effective ionisation rate of the HEXFET can be extracted from the measured breakdown voltage using the assumptions of the dopant concentration and thickness of the drift region. To simplify the analysis, the dopant concentration is assumed to be uniform with abrupt junctions,  $N_A \gg N_D$  and  $dE/dx$  is dependent only on dopant concentration and remains constant at all temperatures. For the 500 V HEXFET, the extracted breakdown electric field profiles at different temperatures are shown in Fig. 6.17(a) following Eqn. 3.24. As temperature decreases, both  $\mathbb{E}_c$  and  $W_{Dm}$  decrease proportionally with constant  $dE/dx$ . The estimated  $\alpha_{eff}$  is extracted from a modification of Eqn. 3.30, where  $g$  remains constant at

## 6.7 Temperature Dependent Breakdown Voltages and Effective Ionisation Rates

7. The results are presented in Fig. 6.17(b). Compared with the calculated  $\alpha_{eff}$  from Fig. 3.20(a), where the change with temperature is expected to increase linearly down to zero kelvin, the extracted  $\alpha_{eff}$  from the measured breakdown voltage of the the 500 V HEXFET is shown to saturate slightly below 100 K where  $\alpha_{eff}(T, \mathbb{E})$  becomes:

$$\alpha_{eff}(T, \mathbb{E}) = (2 \times 10^{-42}T^3 - 1 \times 10^{-39}T^2 + 2.9 \times 10^{-38}T + 3.9 \times 10^{-35})\mathbb{E}^7. \quad (6.24)$$

Eqn. 6.24 is calculated and compared with both the 500 V and 200 V HEXFET measured data. The result are presented in Fig. 6.18(a). The temperature dependent breakdown voltages for higher rated devices were also calculated and the results are presented in Fig. 6.18(b).

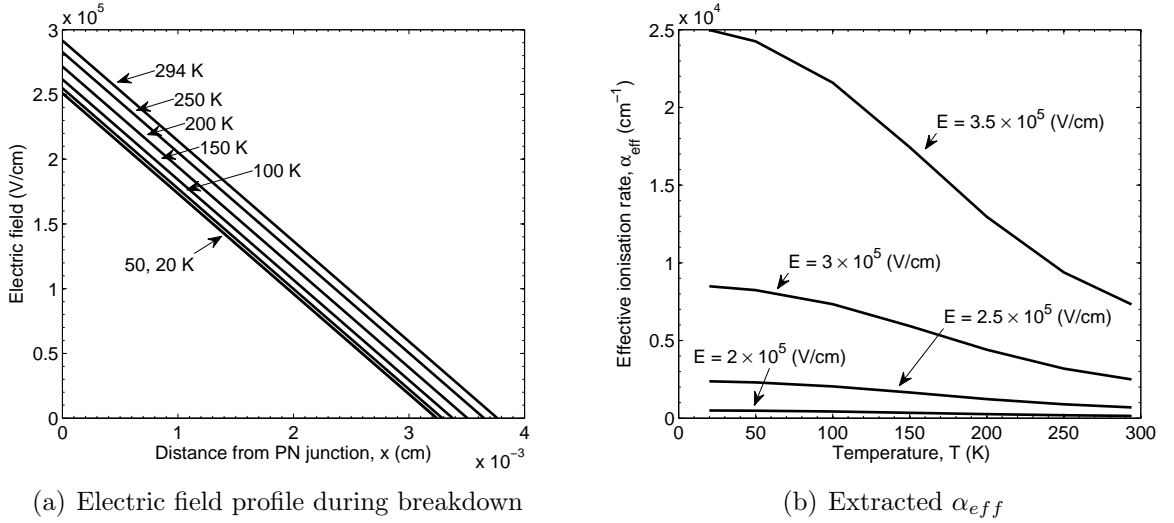


Figure 6.17: (a) The extracted electric field profile during breakdown at different temperatures and (b) the extracted effective ionisation rates at different electric field for the measured 500 V HEXFET.

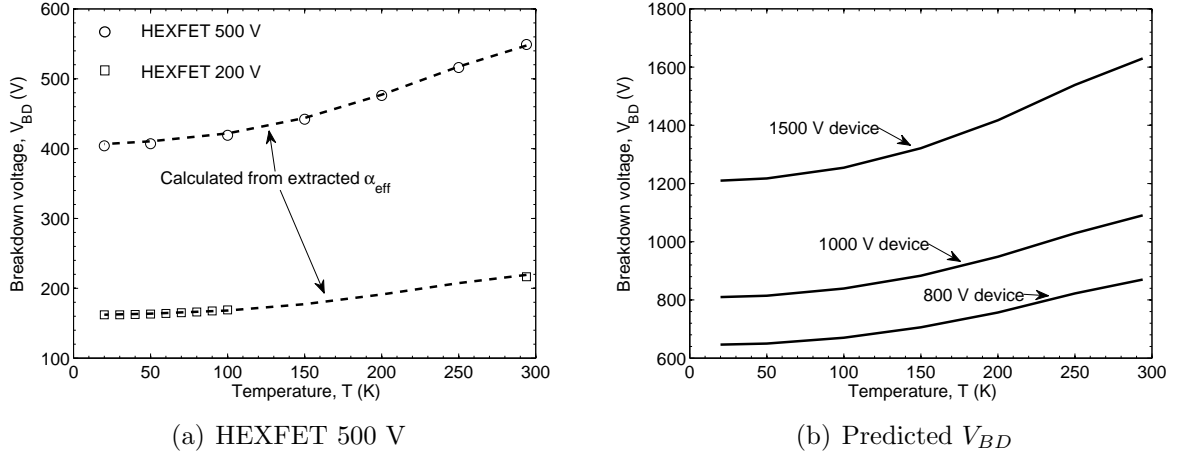


Figure 6.18: (a) Comparison between the measured and calculated  $V_{BD}$  from Eqn. 6.24 for 500 V, 200 V HEXFET and (b) predicted temperature dependent  $V_{BD}$  for higher rated devices.

## 6.8 Breakdown Behaviour Analysis of Super-junction Devices

Despite having a higher drift region dopant concentration, the measured breakdown voltage degradation of the CoolMOS device in Fig. 6.14 was shown to be greater than conventional power MOSFETs. It is likely that the SJ structure is causing this higher degradation rate. Due to many unknown device parameters, such as dopant concentration, pillar width and drift layer thickness, a thorough analysis of the CoolMOS breakdown behaviour would be difficult. Different combinations of these three parameters can achieve the same breakdown voltage, which makes it difficult to accurately extract these parameters. However, by using the extracted temperature dependent effective ionisation rate from Eqn. 6.24, the temperature dependent behaviour of the CoolMOS can be modelled to match the measured behaviour based on trial and error.

Following Strollo and Napoli's analytical model [34], the electric field profile of a SJ device is shown in Fig. 3.19. The profile has two maximum electric field points at diagonal ends of the structure. To simplify the breakdown analysis, the two-dimensional structure can be reduced to a one-dimensional approximation that shows the highest electric field along

## 6.8 Breakdown Behaviour Analysis of Super-junction Devices

the Y direction, this is illustrated in Fig. 6.19. The arrows indicate the decrease in electric field from increasing ionisation rate at lower temperatures. For the purpose of estimating the temperature dependence of the breakdown voltage, the electric field profile can be split into two distinct regions. The first region is the steep electric field on either side of the drift region, similar to the normal electric field profile for a PN junction. The second region is the flat electric field across the middle of the drift region, formed due to the SJ effect. Assuming  $\mathbb{E}_{max,0} = \mathbb{E}_{max,W_{Dm}}$ , the maximum electric field at 300 K,  $\mathbb{E}_{max}(300)$  can be expressed as [34]:

$$\mathbb{E}_{max}(300) = \frac{V_{BD}}{W_{Dm}} + \frac{V_N}{W_{Dm}} L \left( \frac{Y}{W_{Dm}} \right), \quad (6.25)$$

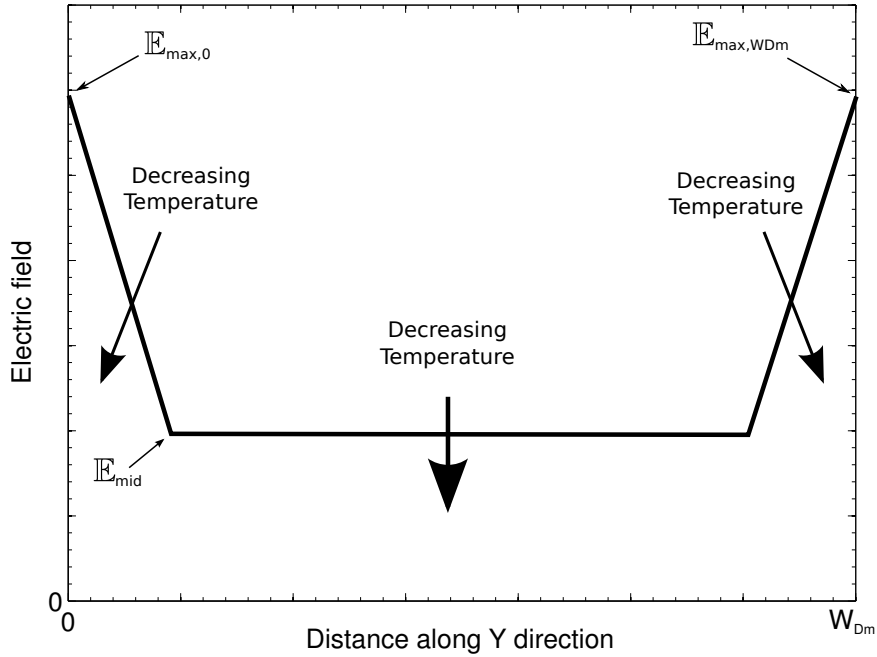


Figure 6.19: An illustration of the one-dimensional breakdown electric field profile of a SJ device.

where  $V_N$  can be approximated as  $(qN_D/\epsilon_0\epsilon_s)W_{Dm}^2$  and  $Y$  is the pillar width.  $L$  is given by the following function:

$$L(t) \simeq 1.697t - 0.7524t^2 - 1.9e - 4t^3, \quad (6.26)$$

## 6.8 Breakdown Behaviour Analysis of Super-junction Devices

where  $t$  is in the range  $0 \leq t \leq 1$ . The electric field in the first region,  $\mathbb{E}(y)$  can be expressed as:

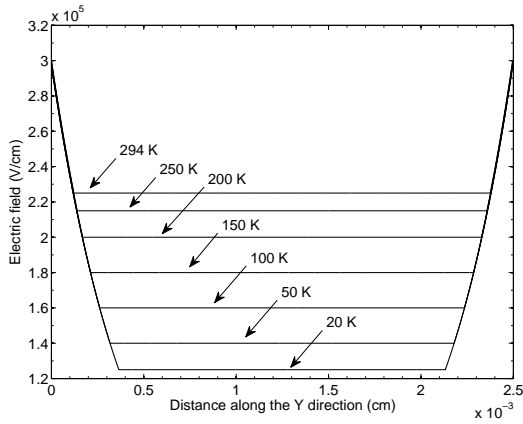
$$\mathbb{E}(y) = \mathbb{E}_{max} \exp \left( -\frac{2y}{L(Y/W_{Dm})W_{Dm}} \right). \quad (6.27)$$

The electric field in the second region at 300 K,  $\mathbb{E}_{mid}(300)$  can be expressed as  $V_{BD}/W_{Dm}$ . The exact temperature dependence of  $\mathbb{E}_{max}$  and  $\mathbb{E}_{mid}$  are unknown but using the extracted effective ionisation rate in Eqn. 6.24, the relationship can be approximated.

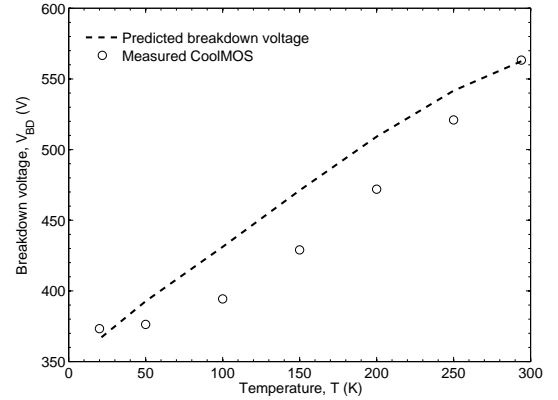
The closest match to the measured CoolMOS data is shown in Fig. 6.20, where  $N_D = N_A = 1.5 \times 10^{15} \text{ cm}^{-3}$ ,  $Y = 5.5 \text{ } \mu\text{m}$  and  $W_{Dm} = 25 \text{ } \mu\text{m}$ . The temperature dependence of  $\mathbb{E}_{max}(T)$  and  $\mathbb{E}_{mid}(T)$  were found to be:

$$\mathbb{E}_{max}(T) = (1.57425 \times 10^{-7}T^2 + 0.00038271 \times 10^{-5}T + 0.885212)\mathbb{E}_{max}(300), \quad (6.28)$$

$$\mathbb{E}_{mid}(T) = (-1.9435 \times 10^{-6}T^2 + 0.00224775 \times 10^{-5}T + 0.511104)\mathbb{E}_{mid}(300). \quad (6.29)$$



(a) Assumed electric field profile



(b) Comparison of the predicted and measured breakdown voltage

Figure 6.20: (a) The assumed temperature dependent electric field profile and (b) the comparison between the predicted and measured breakdown voltage of the 560 V CoolMOS after fitting of  $\mathbb{E}_{mid}(T)$  and  $\mathbb{E}_{max}(T)$ .

The model results show that despite the higher dopant concentration of the drift region, the SJ device can have a higher rate of decrease with lower temperature compared to the conventional drift region. This is due to the two dimensional nature of the electric field



profile of the drift region. However, although the model can predict the general trend of the device, an exact match could not be found. This could be due to a number of reasons. First, the simplified initial assumption of  $\mathbb{E}_{max,0} = \mathbb{E}_{max,W_{Dm}}$  could be inaccurate. In this case, the electric field profile would be altered. Second, the extracted ionisation rate from Eqn. 6.24 may not represent the actual breakdown behaviour of the SJ device since it has a much higher dopant concentration. However, the dopant concentration dependence of effective ionisation rates is relatively unexplored and therefore would require further investigation. Finally, the temperature dependence of  $\mathbb{E}_{max}$  and  $\mathbb{E}_{mid}$  are only an estimation that best matched the analytical model and measured device behaviour. The exact dependence of  $\mathbb{E}_{max}$  with  $\mathbb{E}_{mid}$  and temperature would require the device parameters to be fully known in order to extract their actual dependence.

From Fig. 6.14, the breakdown voltage degradation with lower temperatures was found to be the lowest amongst the MDMesh devices and highest in CoolMOS devices. Even though both devices are SJ based structures, the two temperature dependencies are quite different. The most likely reason for this difference is the semi-SJ structure of the MDMesh device. As stated in Chapter 5.1.3, the P-type pillars in MDMesh do not reach all the way down to the substrate and there is a one dimensional drift region underneath the SJ structure. Depending on the dopant concentration of this layer, the depletion layer may reach the substrate, making it a punch-through or non-punch-through structure. This is shown in Fig. 6.21 as an exaggerated illustration of the electric field profile of the MDMesh device. If the dopant concentration of the one dimensional drift layer,  $N_{D-1D}$  is much lower than the dopant concentration of the SJ structure,  $N_{D-SJ}$ . In this case,  $\mathbb{E}_{max,0} \neq \mathbb{E}_{max,W_{SJ}}$ , this will likely lead to a lower  $\mathbb{E}_{mid}$ . However, due to the punch through effect of the one dimensional drift layer, the breakdown voltage degradation could be spread across both  $\mathbb{E}_{mid}$  and the electric field across the drift region. This will result in a lower degradation at lower temperatures in comparison to a conventional SJ device. A disadvantage of this structure is that by having the extra lower doped drift layer, this results in a higher on-state resistance. This could explain why MDMesh has the highest on-state resistance in the comparative analysis in Chapter 5.1.4. However, as discussed in the previous section, operating power

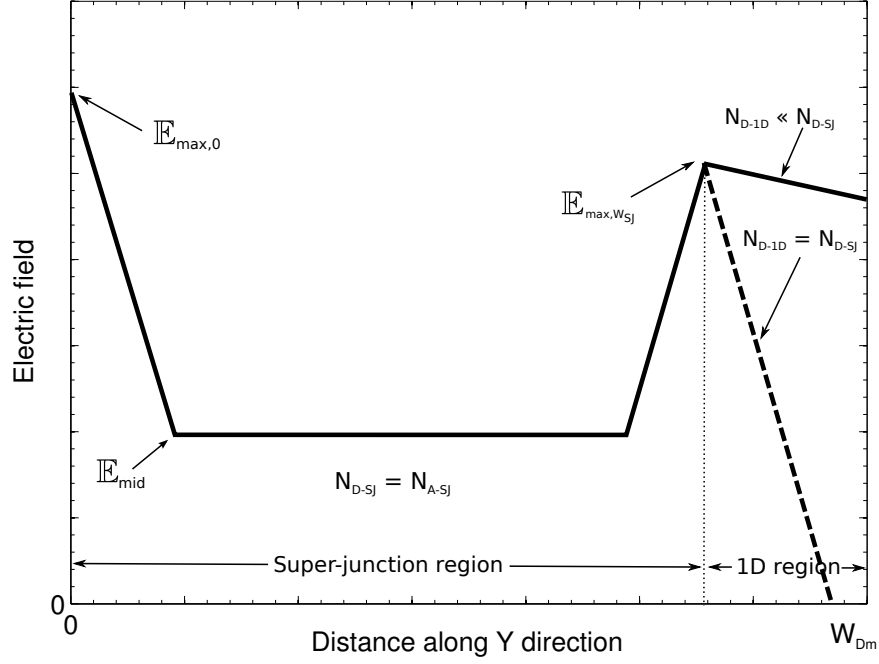


Figure 6.21: An exaggerate illustration of the electric field profile of a semi-SJ device.

MOSFETs at cryogenic temperatures would require a higher room temperature breakdown voltage, which would result in an increase in the on-state resistance. Therefore, there could be a trade-off between using semi-SJ devices to obtain a higher breakdown voltage at cryogenic temperatures and simply using a higher rated breakdown voltage device.

## 6.9 Super-junction Device Optimisation for $T < 50$ K Operation

As shown in chapter 5.1, one of the main problems with power MOSFETs operating at temperatures below 50 K is the large variation of the on-state resistance between identical devices. In section 6.5, it was proposed that the reason behind this behaviour is due to the free carrier concentration sensitivity to the background doping concentration of the JFET region near the surface of the oxide interface. In order to validate this theory, further experiments must be performed to measure the devices with different known background doping concentration of the JFET region. If this theory is validated, the on-state resistance

## 6.9 Super-junction Device Optimisation for $T < 50$ K Operation

variation problem can be mitigated by careful control of the doping concentration of the JFET region.

As discussed at the end of section 6.5, although the average CoolMOS on-state resistance was higher than the HEXFET devices, CoolMOS 1 did exhibit the lowest on-state resistance out of all the measured devices. If the on-state resistance variation problem can be mitigated by careful control of the doping concentration of the JFET region, then it may be possible to further optimise SJ devices to operate at temperatures below 50 K. However, as discussed in section 6.8, the measured breakdown voltage degradation of the CoolMOS devices were shown to be greater than conventional power MOSFETs. Therefore, in order to increase the breakdown voltage capability of the SJ device, it may be advantageous to reduce the dopant concentration of the drift region. In addition, the electron mobility would also increase. Following Strollo and Napoli's analytical model [34], the theoretical effects of reducing the dopant concentration on breakdown voltage can be seen in Fig. 6.22. All the parameters have been previously defined in section 6.8.

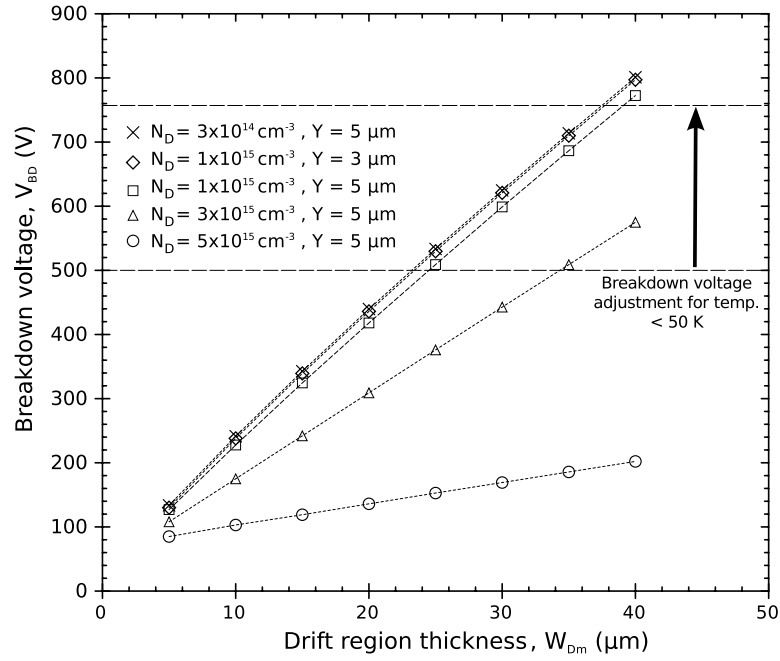


Figure 6.22: The calculated breakdown voltage of the SJ structure in relation to the drift region thickness for five dopant concentration ( $N_D$ ) and pillar width ( $Y$ ) combinations. The lines show the  $W_{Dm}$  adjustment required to achieve a 500 V breakdown structure for temperatures below 50 K.

## 6.9 Super-junction Device Optimisation for $T < 50$ K Operation

For a 500 V SJ device, with  $N_D = 3 \times 10^{15} \text{ cm}^{-3}$  and  $Y = 5 \text{ } \mu\text{m}$ , the required  $W_{Dm}$  is  $\sim 35 \text{ } \mu\text{m}$ . Assuming there is an over all  $\sim 34 \%$  reduction in  $V_{BD}$  for a higher voltage rated device down to 50 K from room temperature, in order to achieve 500 V for  $V_{BD}$  at temperatures below 50 K,  $N_D$  can be reduced to  $1 \times 10^{15} \text{ cm}^{-3}$  and  $W_{Dm}$  increased to  $\sim 39 \text{ } \mu\text{m}$  in order to sustain a  $V_{BD}$  of 785 V at room temperature. The same result can be achieved by keeping  $N_D$  at  $3 \times 10^{15} \text{ cm}^{-3}$  and increasing  $W_{Dm}$  to  $5.7 \times 10^{-3} \text{ cm}$ . Further reduction in  $N_D$  is possible, however, this will reduce the free electron concentration considerably and the improvement in  $V_{BD}$  is relatively low.

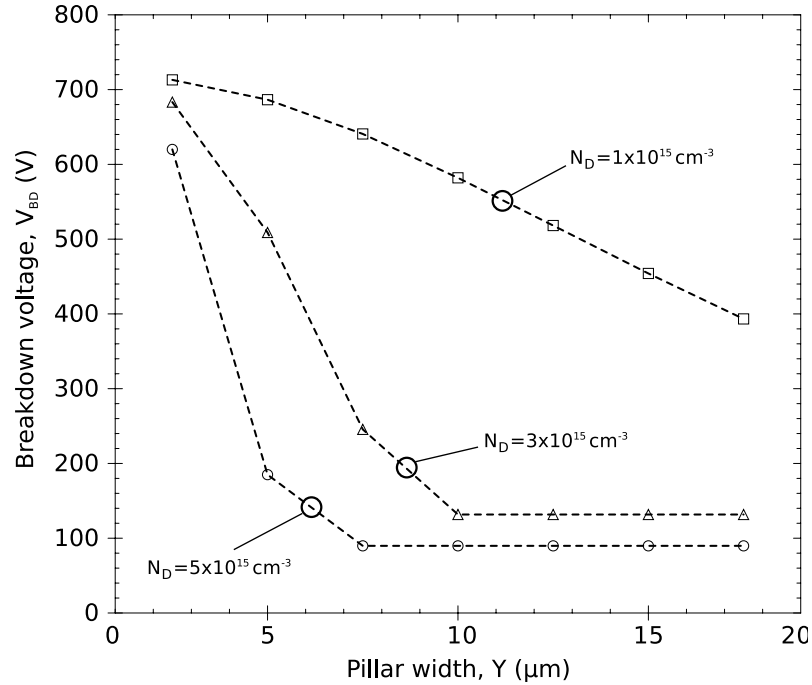


Figure 6.23: The calculated breakdown voltage of the SJ structure in relation to the pillar width for three different dopant concentration.

As shown in Fig. 6.22, the  $V_{BD}$  achieved with  $N_D = 3 \times 10^{14} \text{ cm}^{-3}$  and  $Y = 5 \text{ } \mu\text{m}$  can also be achieved with  $N_D = 1 \times 10^{15} \text{ cm}^{-3}$  and reducing  $Y$  to  $3 \text{ } \mu\text{m}$ . The effectiveness of reducing  $Y$  is dependent on the dopant concentration. As shown in Fig. 6.23, reducing  $Y$  is much more effective with higher  $N_D$  and low  $Y$  values. If  $Y$  is too high, then the charge compensation effect of the SJ structure becomes lost. At lower  $N_D$ , the gradient of reducing  $Y$  with increasing  $V_{BD}$  is less steep. However, in reality there is a limit to how small the

## 6.9 Super-junction Device Optimisation for $T < 50$ K Operation

manufacturers can control  $Y$ , so  $Y$  is a difficult parameter to reduce significantly.

By adjusting the design parameter of the SJ device to achieve the required  $V_{BD}$ , the on-state resistance will also be affected. At  $T \leq 50$  K, the temperature dependent specific on-state resistance of the SJ drift layer is given by:

$$R_{drift} = \frac{2W_{Dm}}{q\mu_n(T)n(T)}. \quad (6.30)$$

The specific drift region resistance of a symmetric SJ device is twice the resistance of the N pillar [34]. The calculated results on the specific on-state resistance by the adjusted parameters to achieve  $V_{BD} = 500$  V at  $T \leq 50$  K are shown in Fig. 6.24. In comparing the two options of either reducing  $N_D$  to  $1 \times 10^{15} \text{ cm}^{-3}$  and increasing  $W_{Dm}$  by  $4 \times 10^{-4} \text{ cm}$  or keeping  $N_D$  the same and increasing  $W_{Dm}$  by  $22 \text{ } \mu\text{m}$ , the former option appears to have a lower on-state resistance at  $T \leq 50$  K.

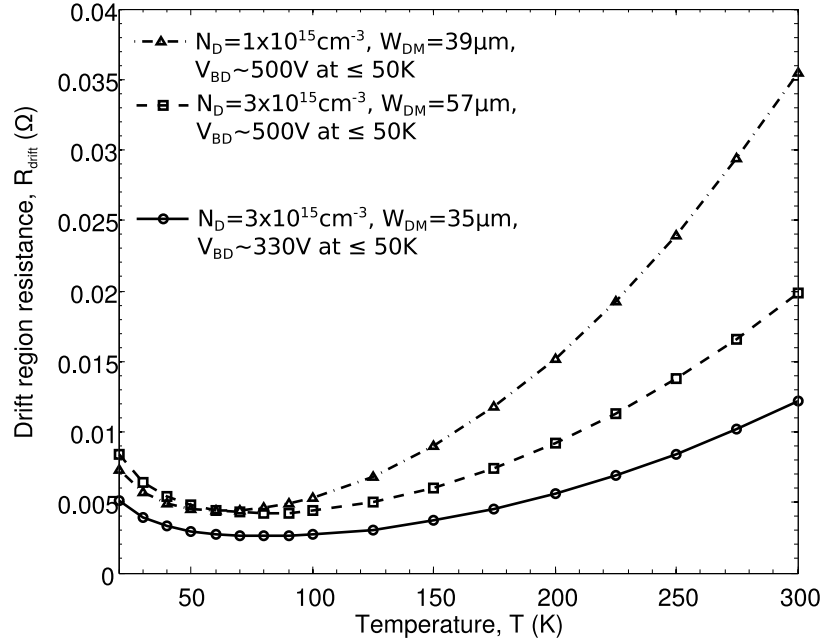


Figure 6.24: The calculated temperature dependent specific on-state resistance of the drift layer for the two adjusted SJ structure to achieve 500 V breakdown voltage for  $T < 50$  K, the on-state resistance of the original 500 V SJ device at room temperature is also added for comparison.

## 6.10 Conclusion

This chapter analyses the measured cryogenic behaviour of the various power MOSFETs by interpreting the behaviour through known theories and calculations. In terms of the on-state resistance, at temperatures above the carrier freeze-out range, the main parameter that dominates  $R_{ON}$  was found to be the electron mobility within the drift region. Within the carrier freeze-out range, generally  $<50$  K, it was suggested that the main parameter that dominates  $R_{ON}$  at low voltage is the initial free carrier concentration. This is controlled by the background dopant concentration in the accumulation layer underneath the oxide surface. In terms of the breakdown behaviour, the temperature dependent  $\alpha_{eff}$  was extracted from the measured MOSFETs. This can be used to predict the temperature dependence of other power MOSFETs at cryogenic temperatures. The breakdown behaviour of SJ devices was also analysed and semi-SJ devices were found to have the lowest degradation rate at cryogenic temperatures. Furthermore, it is proposed that SJ devices can be further optimised for cryogenic operation below 50 K by changing a combination of variables such as:  $N_D$ ,  $W_{Dm}$  and  $Y$ .

# Design of the Free-wheeling Demonstration Circuit

The final objective of this study is to demonstrate an operational prototype model, which uses power devices to control the free-wheeling current for a HTS inductor coil at a temperature of 30 K (See chapter 1.2). The core requirements for the power devices were required to be gate controllable, operational at 30 K, exhibit very low power losses and have a sufficient voltage blocking capability. From the conclusions in chapter 5.5, a silicon n-channel power MOSFET was suggested as the best device candidate for this application.

Power MOSFETs are voltage controlled devices, making the gate control relatively easy and fast. Unlike the IGBT or Thyristor, they do not have forward threshold voltages which limit the voltage drop during conduction. Furthermore, by parallelling power MOSFETs, the current rating increase and consequently the forward voltage decrease. This is especially useful when low power losses are critical for the stability of the cryogenic system.

## 7.1 Circuit Configuration

For the demonstration model, the basic free-wheeling circuit design is presented in Fig. 7.1. The power devices used to control the free-wheeling current in cryogenic conditions will be a pair of power MOSFETs connected back-to-back in series. This configuration enables the MOSFETs to block bi-directional voltage in the off state. The top power MOSFET

## 7.1 Circuit Configuration

is required to block current flowing through the MOSFETs during “start up” mode and during the short voltage pulses in “top up” mode (see chapter 1.2). The bottom MOSFET is necessary during “protection” mode to stop current flowing back into the HTS coil during a quench event. This will force the current to discharge via the diodes outside the cryogenic chamber. With the back-to-back configuration of the two power MOSFETs, their source terminals will be tied together. This means that the gate voltage for either of the gates will have to be positively biased to the same point. This means that if both power MOSFETs can be simultaneously controlled then only one gate drive would be required and the gate control can be simplified.

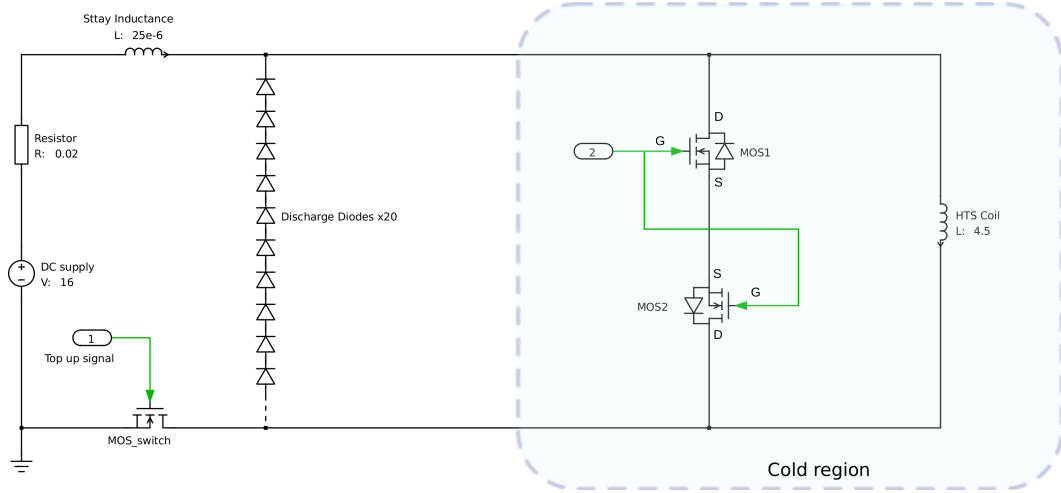


Figure 7.1: The basic circuit design of the demonstration model with back-to-back MOSFETs as the free-wheeling device.

Other than the back-to-back MOSFETs and HTS coil, the remainder of the circuit is situated outside the cryo-chamber at room temperature. A voltage supply of 16 V is used to charge the HTS coil through a 20 mΩ series resistor. There are twenty commutation diodes in series for current discharge in parallel with the HTS coil. The reverse voltage has to reach at least 20 V before the diodes can begin conducting. The charging sequence is controlled by a low side power MOSFET. Due to the long wiring between the voltage supply and the commutation diodes, an estimated stray inductance of 25 μH is expected. This will result in high voltage overshoot during switching events of the low side power MOSFET. Reducing



the stray inductance in this situation would be problematic. Also, since the switching speed in this application is not crucial, a high gate resistance could be used to slow down the switching speed of the low side MOSFET in order to avoid high voltage stress. The required gate resistance was calculated to be  $\sim 1\text{ k}\Omega$ , which should give a manageable turn off voltage overshoot of  $\sim 15\text{ V}$ . The slow turn-off time is calculated to be approximately  $150\text{ }\mu\text{s}$ . In order to avoid shoot-throughs, dead-times are required between the switching of the low side MOSFET and the back-to-back MOSFETs (especially during turn-off). An appropriate dead-time would be  $50\text{ }\mu\text{s}$ , this would ensure the complete turn-off of the low side MOSFET.

## 7.2 Power MOSFET Selection

With the back-to-back MOSFETs configuration, the on-state series resistance of the system would be doubled. Therefore, it is necessary to maximise the number of power MOSFETs in parallel or increase the current ratings of the devices to reduce the power losses. In this case, a number of small power MOSFETs in parallel would not be the best solution. Rather, using a power MOSFET module with high current rating would simplify the gate wiring and spacing limitations. A good power MOSFET module for this application in terms of voltage/current ratings, spatial dimension and on-state resistance was found to be the IXYS - PolarHT™ Module (VMO 1600-02P). A 200 V, 1900 A (at  $25^\circ\text{C}$ ) rated,  $1.7\text{ m}\Omega$  typical  $R_{ON}$ , single n-channel enhancement mode power MOSFET. See appendix C for further information.

In order to operate this power MOSFET module at cryogenic temperatures, it should first be characterised. However, due to the limited spacing inside the cryogenic characterisation system introduced in chapter 4, it is not possible to fit the full module within the small chamber. A much larger cold-head/chamber would be required to accommodate the large power module. Nevertheless, there are smaller current rated PolarHT devices in the TO-264 package that would fit the cold-head, they are the (IXTK 140N20P) 200 V and 140 A rated,  $18\text{ m}\Omega$  typical  $R_{ON}$ . Assuming the same die were used in both packages but scaled up for the higher current rated power MOSFET module, the cryogenic behaviour of the PolarHT

power MOSFET can then be characterised.

Three identical PolarHT (IXTK 140N20P) samples were chosen and are designated as H1, H2 and H3. The forward and reverse IV characteristics for H3 are presented in Fig. 7.2 at  $V_{GS} = 15$  V. The measurement at 30 K is highlighted with red to differentiate it from higher temperature measurements. The figure shows that if the reverse voltage does not reach the threshold voltage of the reverse body diode, the IV characteristics of the first quadrant is inversely identical to the third quadrant at all temperatures. This is important since the top power MOSFET will only operate in the third quadrant during free-wheeling operation.

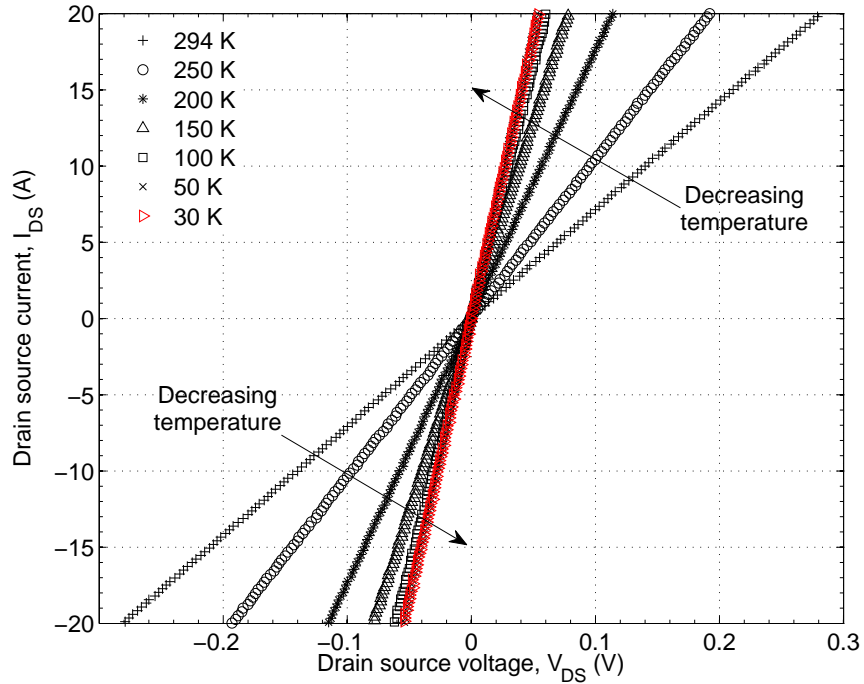


Figure 7.2: The forward and reverse IV characteristics of PolarHT (IXTK 140N20P), sample H3, at  $V_{GS} = 15$  V.

Fig. 7.3 presents temperature dependent on-state resistance data for all three samples at  $V_{GS} = 15$  V. Surprisingly, both H1 and H3 exhibited their lowest on-state resistance at  $\sim 40$  K which is much lower than other measured power MOSFETs. The reduction in the on-state resistances are less than 20 % of the value at room temperature. Furthermore, H2 exhibited

no observable carrier freeze-out effects even at 20 K. Overall, the on-state resistances for all three devices between 30 K and 60 K were relatively insensitive to temperature changes. More importantly, non-ohmic behaviour was not observed in any of the measured PolarHT devices.

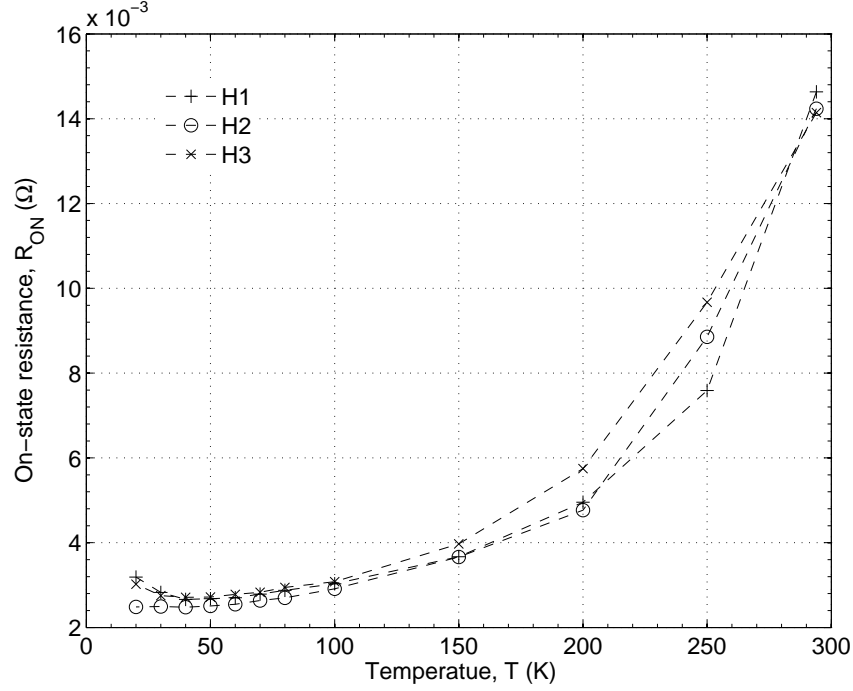


Figure 7.3: The temperature dependent on-state resistance of the three measured PolarHT power MOSFETs.

The temperature dependent breakdown voltages at 250  $\mu$ A for all three devices are presented in Fig. 7.4. Both H1 and H3 exhibited non-isotropic behaviour. For H1, the breakdown voltage was found to increase as temperature was reduced from 30 K to 20 K. For H3, the breakdown voltage increased as temperature was reduced from 40 K to 20 K. These were the only measured power MOSFETs that exhibited non-isotropic behaviour for the breakdown voltage. The reason for this behaviour is uncertain. However, since H2 did not exhibit any non-isotropic behaviour, this behaviour may not occur in all PolarHT devices. On average, the breakdown voltage of the three power MOSFETs was 25 % lower at 30 K than at room temperature.

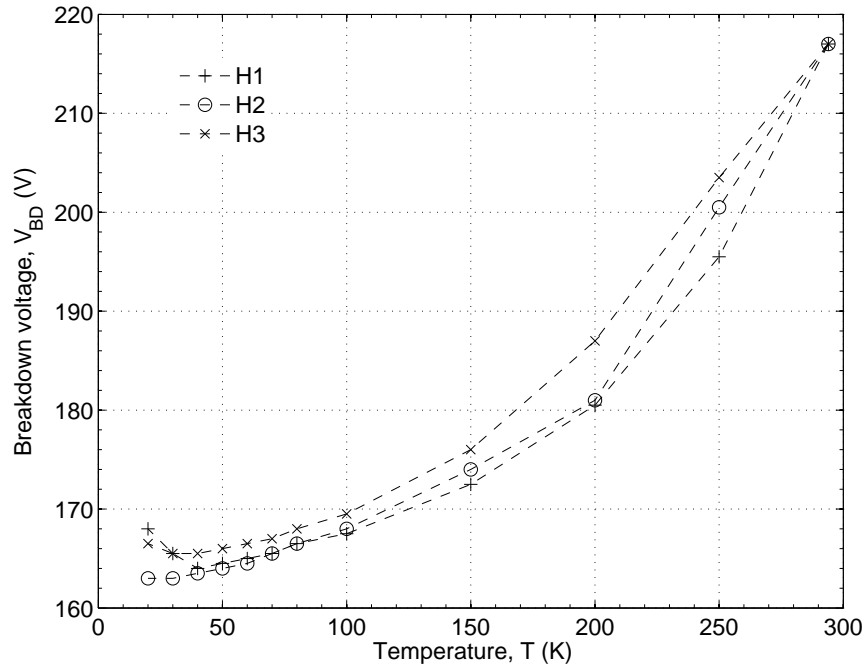


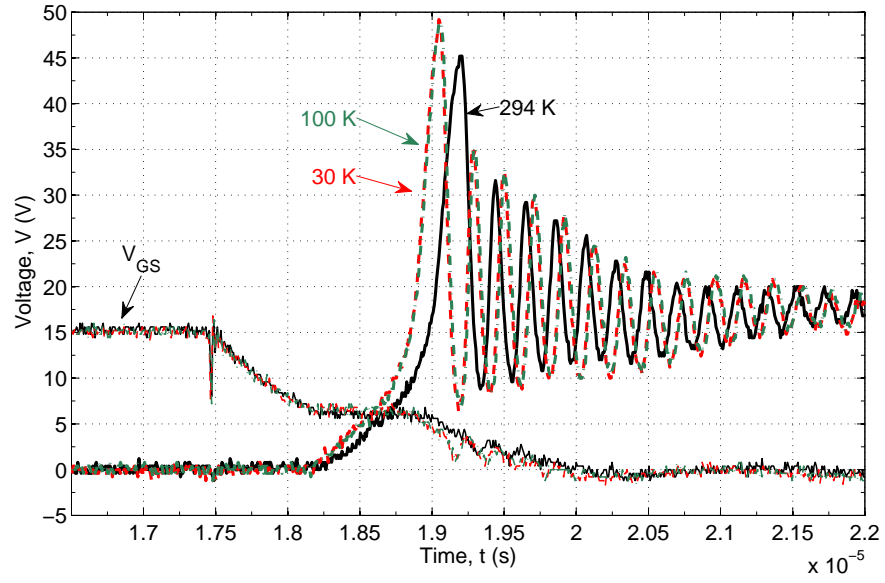
Figure 7.4: The temperature dependent breakdown voltages of the three PolarHT devices.

The PolarHT voltage switching waveforms for H3 are presented in Fig. 7.5. The turn-off waveforms exhibited increased voltage overshoot as well as early onset of device during turn off at 100 K and 30 K compared to the room temperature measurement. In fact, the measurements for the two temperature points were almost identical. The turn-on waveforms exhibited delayed turn-on at cryogenic temperatures. This behaviour follows the temperature dependence found in the switching measurements of the HEXFETs in chapter 5.1. Although, the voltage overshoots for the PolarHT devices were lower than for the HEXFETs.

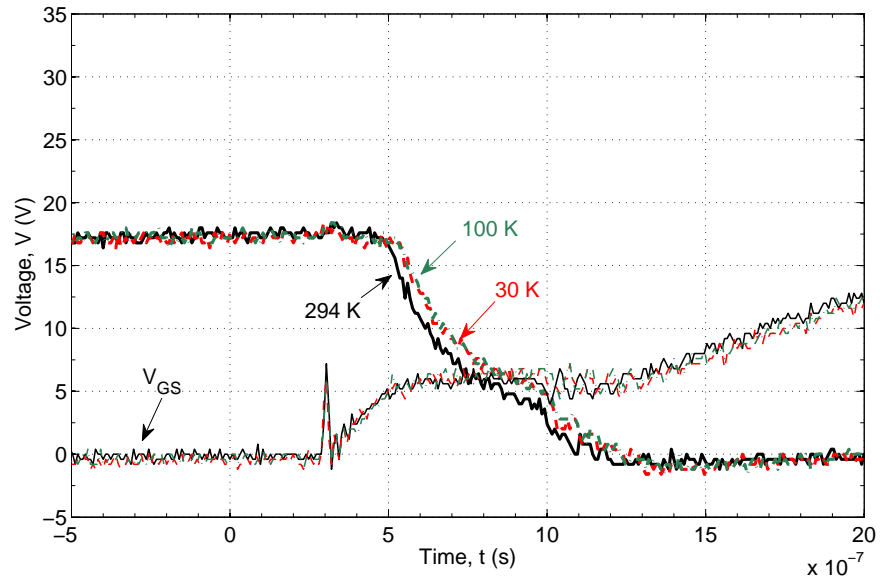
The presented data have shown that the polarHT MOSFET devices are likely to be suitable for cryogenic operation. It has good on-state resistance properties at the required operating temperature and sufficient breakdown voltage capability.

### 7.2.1 Silicone Gel Removal

As discussed in chapter 2.2, it is known that the silicone gel commonly used in power modules becomes crystalline at temperatures below  $-50^{\circ}\text{C}$  (223 K). Therefore, it is essential



(a) Turn-off voltage



(b) Turn-on voltage

Figure 7.5: The temperature dependent (a) turn-off and (b) turn-on voltage waveforms at 294 K, 100 K and 30 K for the PolarHT MOSFET (H3). The gate voltages are also presented for reference.

for the operation of this demonstration model that all the silicone gel inside the PolarHT power MOSFET module is removed before subjecting it to cryogenic temperatures. For this

application, removing the dielectric material is acceptable because protection from arcing is providing by the high vacuum/low pressure environment due to the Paschen's law [108]. However, the modules will have to be protected from dust and other contaminates even during storage.

A common practice to remove silicone gel is to use a silicone de-polymeriser solution such as Digesil® NC. However, after opening the module, it was discovered that there is also an epoxy layer on top of the silicone gel which blocks access to the gel. In order to gain access to the silicone gel for the de-polymeriser solution to operate, two  $2 \times 2 \text{ cm}^2$  hole pockets were milled out of the epoxy layer. The epoxy layer was found to be 4 mm thick and covers the entire surface of the module. See appendix B for illustrations.

## 7.3 Circuit Simulation

In order to fully understand the operation of the demonstration circuit in all modes of operation, the circuit was simulated using the Piecewise Linear Electrical Circuit Simulation (PLECS) software. The first of the circuit's four modes of operations is "start up" mode, where the field current of the HTS coil is charged from 0 A to 135 A. "free-wheeling" mode is where the current flows around the back-to-back MOSFETs and HTS coil path indefinitely, separate from the external power source. "Top up" mode is where the field current is recharged to the maximum current of 135 A by switching on the low side MOSFET and turning off the back-to-back MOSFETs for a short period of time. This occurs when the free-wheeling current decays below an arbitrary minimum value (130 A). Finally, "protection" mode is where the field current in the HTS coil is shunt to the twenty commutation series diodes. The diodes will activate when the voltage across the HTS coil becomes higher than -20 V.

Since the on-state resistance of the PolarHT module at 30 K cannot be measured with the cryogenic rig, the value will have to be estimated from the measured smaller PolarHT samples. The average on-state resistance for the three PolarHT (IXTK 140N20P) samples at 30 K is  $2.69 \text{ m}\Omega$  with  $V_{GS} = 15 \text{ V}$ . Since each device contains one die, it is estimated that

the PolarHT module (VMO 1600-02P) would contain 14 dies in parallel to support 1900 A at 25°C. Assuming current will be shared equally amongst the 14 dies, this would give an estimated on-state resistance of 0.192 mΩ for the MOSFET module at 30 K. The on-state resistance changes very little between 30 K up and 60 K, therefore the on-state resistance can be assumed to be constant over this temperature range. The HTS coil is assumed to have an inductance value of 4.5 H and the discharge diodes are assumed to have a threshold voltage of 1 V.

### 7.3.1 Control of Back-to-back MOSFET with a Single Gate Driver

This first models analyse a single gate driver controlling both the back-to-back MOSFETs simultaneously in order to evaluate whether any fast voltage transient would occur in the series diodes. The full circuit schematic is presented in Fig.7.6.

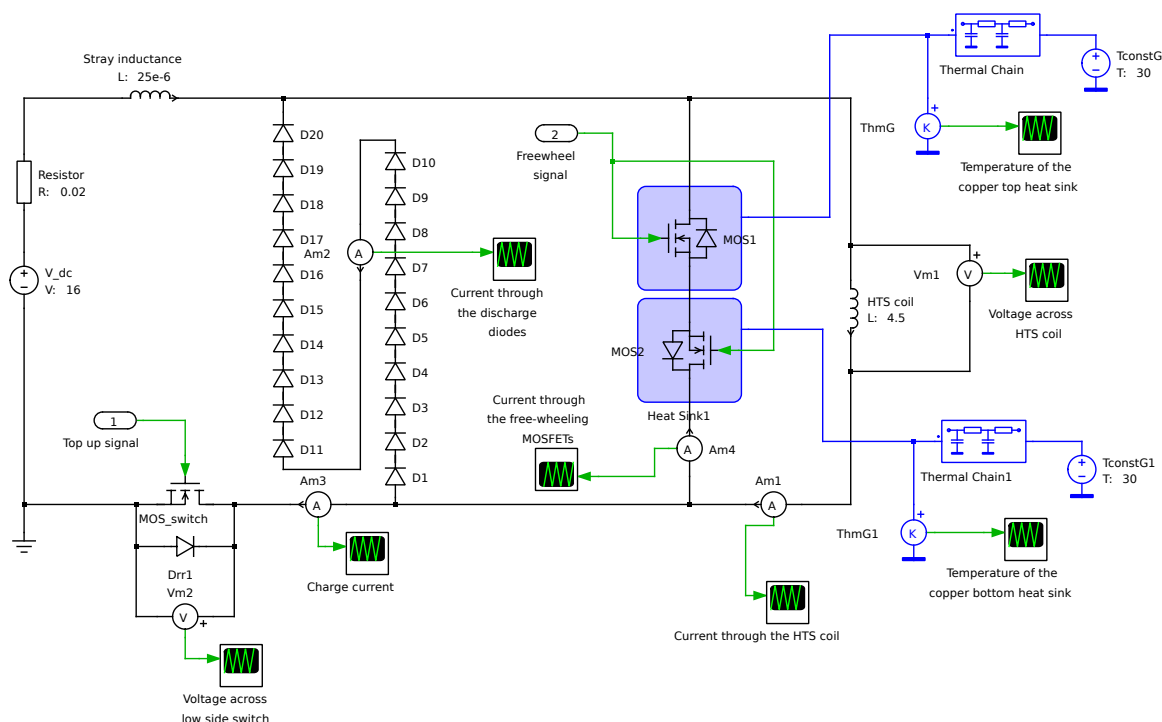


Figure 7.6: Simulation circuit in PLECS.

The “start up” mode can be seen in Fig. 7.7(a). At the voltage supply of 16 V, the circuit took 42 seconds to charge the HTS coil from 0 A to 135 A. During “free-wheeling” mode,

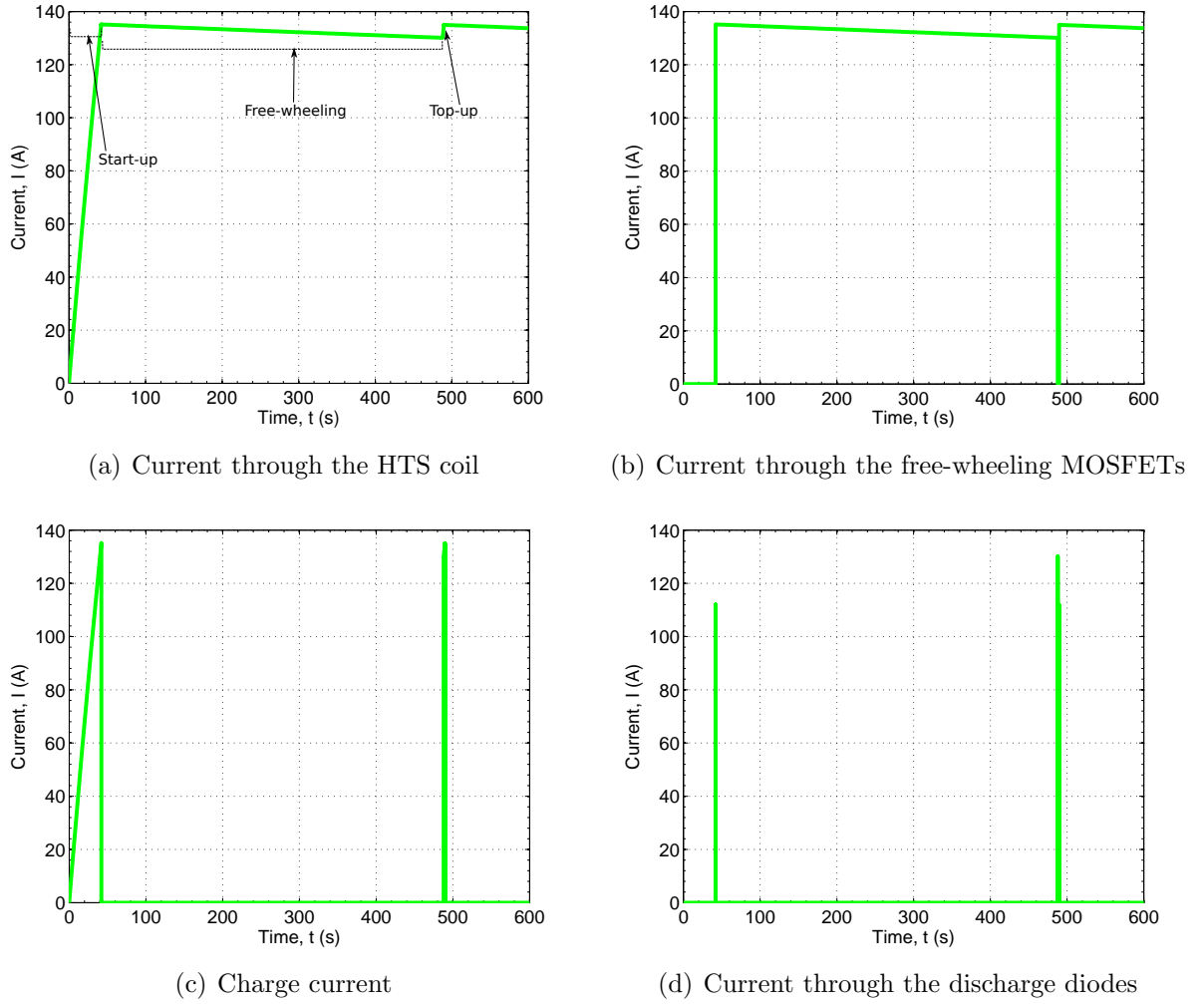
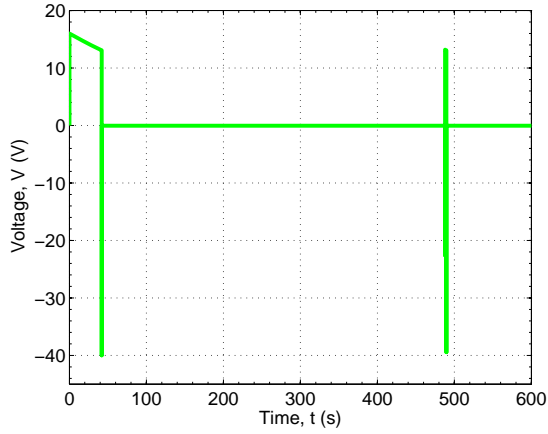


Figure 7.7: The simulated current results from the demonstration circuit in Fig. 7.6.

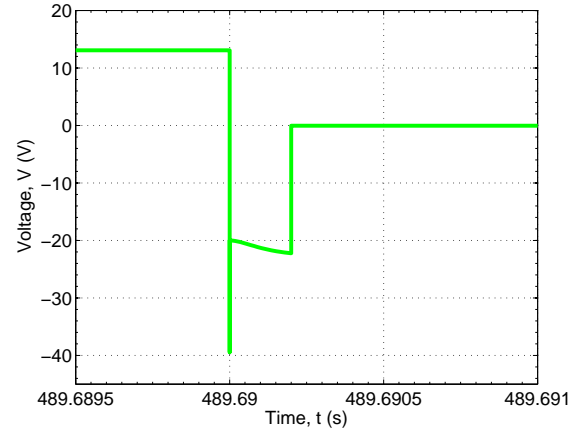
the free-wheeling current took approximately 7.5 minutes to decay from 135 A to 130 A and during “top up” mode it took 1.7 seconds to recharge back from 130 A to 135 A. Assuming indefinite operation, this would mean that the circuit would be required to recharge eight times an hour with topping up time taking only 0.38% of each cycle. Fig. 7.7(b) shows the current through the free-wheeling back-to-back MOSFETs. The ultra loss power MOSFETs were able to maintain the field current for long periods of time. Fig. 7.7(c) shows the charging current through the low side MOSFET, the data shows the long start up ramp current and a small burst of top up current required to maintain the free-wheeling current above 130 A. Fig. 7.7(d) shows the current discharged through the diodes during the dead-



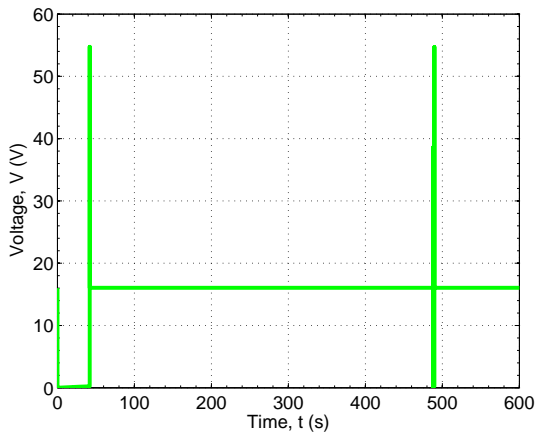
times between the start-up and free-wheeling modes, as well as the switching events between free-wheeling and top-up modes.



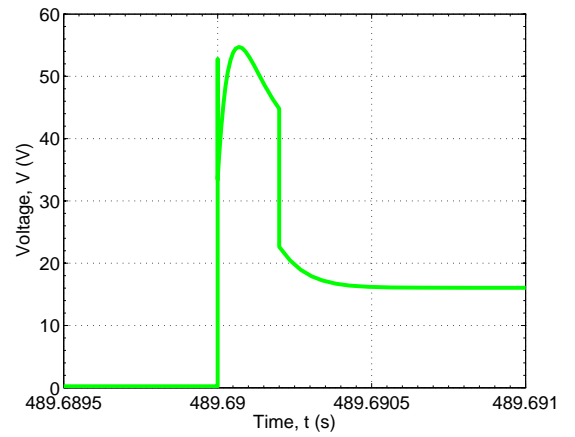
(a) Voltage across the HTS coil



(b) Voltage across the HTS coil during the end of top-up mode



(c) Voltage across the low side switch



(d) Voltage across the low side switch during the end of top-up mode

Figure 7.8: The simulated voltage results from the demonstration circuit shown in Fig. 7.6.

The voltage across the HTS coil is shown in Fig. 7.8(a), it shows the voltage undershoot during the turn-off of the low-side MOSFET. The undershoot was higher than expected, mainly due to the fast voltage transients from the series diodes. Fig. 7.8(b) shows the zoomed in view of the voltage across the HTS coil during the turn-off of the low side MOSFET. After the high voltage spike, the voltage stays above 20 V due to the short current discharge across the series diodes during the dead-time period. In the free-wheeling periods, only the voltage

across the back-to-back MOSFETs can be seen by the HTS coil. Fig. 7.8(c) shows the voltage across the low side MOSFET, it shows the high voltage overshoot due to the simulated stray inductance, in addition to the voltage across the series diodes. Fig. 7.8(d) shows the zoomed in view of the voltage across the low-side MOSFET during the turn-off event.

The thermal behaviour of the back-to-back MOSFETs was also simulated, by assuming each power MOSFETs is thermally connected to a copper heatsink that is also thermally connected to a constant 30 K temperature source. Each copper heatsink was assumed to have dimensions of approximately  $79 \times 62 \times 7$  mm and a mass of 300 grams and completely covers the bottom copper base plate of the module. The thermal conductivity of copper at 30 K is assumed to be 2140 W/mK and specific heat capacity at 30 K is 26.4 J/kgK. The simulated temperature of the heatsink is presented in Fig. 7.9, the increase in temperature due to the power loss from each power MOSFET is negligible at 30 K.

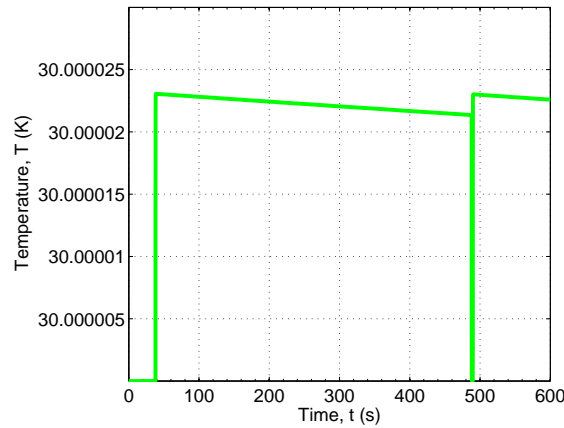


Figure 7.9: Simulated temperature of the top copper heatsink from Fig. 7.6.

For “protection” mode, both the low side MOSFET and the back-to-back MOSFETs were switched off at 135 A (straight after a top up event) in order to force the free-wheeling current to discharge via the commutation series diodes. The simulated discharge current and voltage waveforms are shown in Fig. 7.10(a) and 7.10(b) respectively. Assuming each series diode has a threshold voltage of 1 V and 1 mΩ on-state resistance, the figures show that it would take approximately 28 seconds to discharge all the current from the HTS coil from 135 A. However, this assumes the temperatures of the diodes doesn’t change. The voltage

overshoot was kept below -40 V, well within the voltage blocking capability of the power MOSFETs.

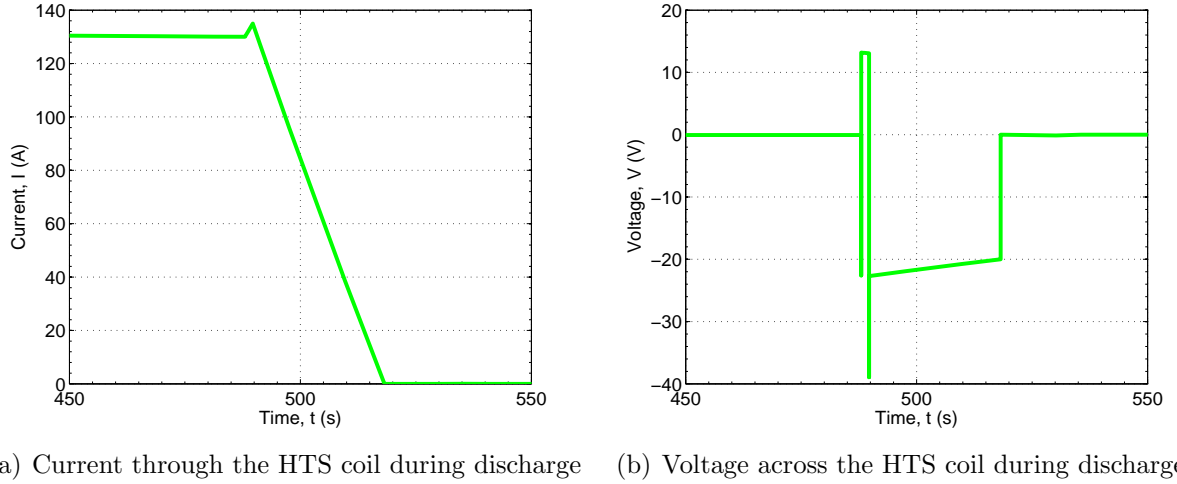


Figure 7.10: The discharge current and voltage waveforms from Fig. 7.6.

#### 7.3.2 Avoiding Fast Voltage Transients

Up to this point, the back-to-back MOSFETs were assumed to be controlled simultaneously by a single gate driver. However, as shown in the last section, during the turn-off of the low-side MOSFET, high voltage spikes occur and the commutation diodes conduct for short periods of time. This could cause them to snap quite badly due to the fast voltage transients, which could cause further voltage spikes during their turn-off event. One possible and simple approach to mitigate these effects is to leave the bottom gate on constantly through out all the modes, except during “protection” mode. This will ensure the current can continue to flow through the back-to-back MOSFET path via the body diode of top MOSFET. This will limit the fast voltage transients and stop the commutation diodes from turning on during the dead-times. In this arrangement, the top and bottom MOSFETs will have to be controlled separately, with the bottom MOSFET only turning off in the event of a quench. However, this would mean that the top MOSFET would dissipate short bursts of heat during the short dead-time periods from the conduction of the body diode. The gate signals for the three

MOSFETs for all four modes are illustrated in Fig. 7.11 and the new simulated circuit with the split control for the top and bottom MOSFETs is shown in Fig. 7.12.

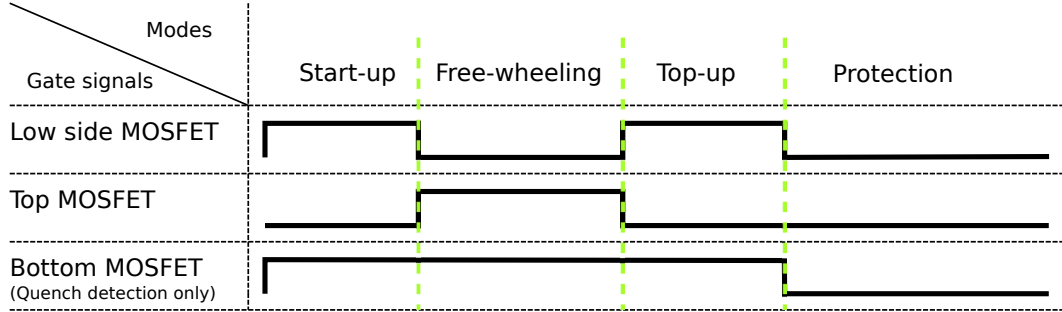


Figure 7.11: The gate signals for all four modes of operation.

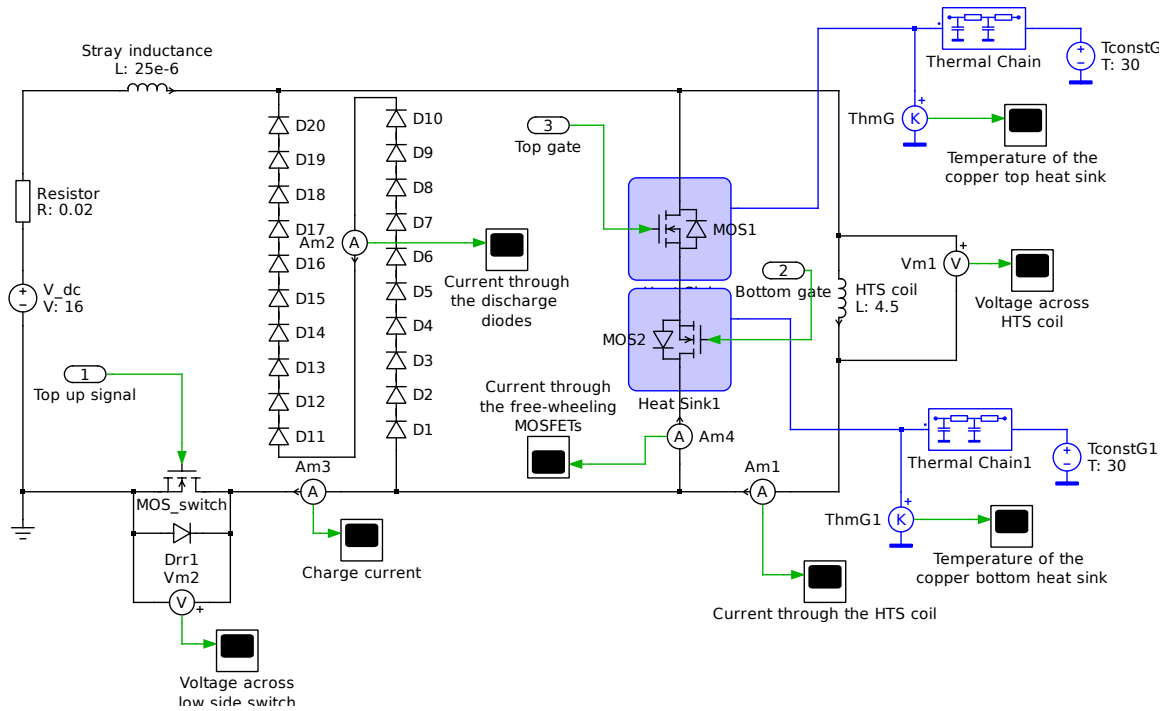
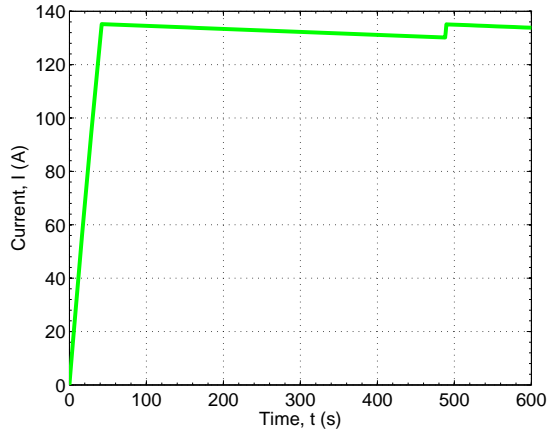
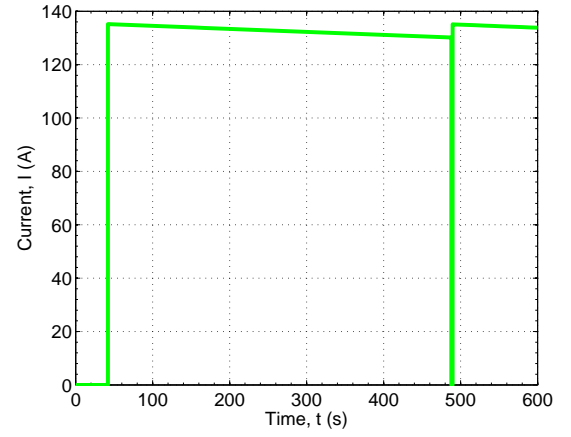


Figure 7.12: Simulated circuit with split control for the top and bottom MOSFETs.

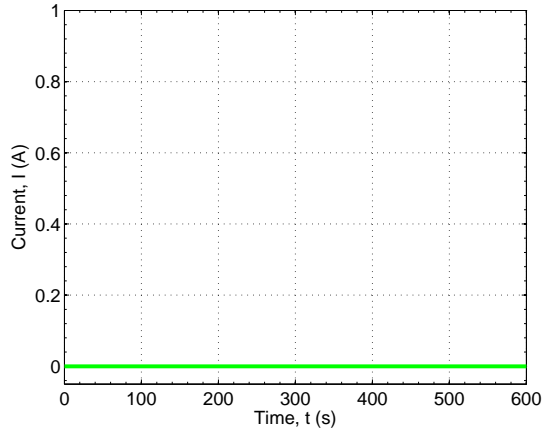
The simulated current through the HTS coil is shown in Fig. 7.13(a). With the new arrangement the “start up” mode took the same amount of time to charge the HTS coil from 0 A to 135 A as before. Fig. 7.13(b) shows the current through the back-to-back MOSFETs was not affected by the new split gate control of the top and bottom MOSFETs.



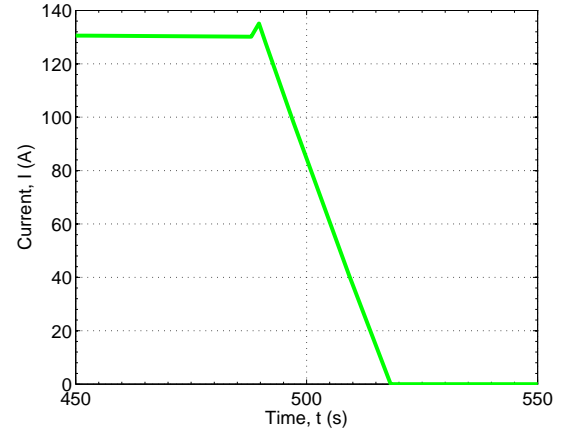
(a) Current through the HTS coil



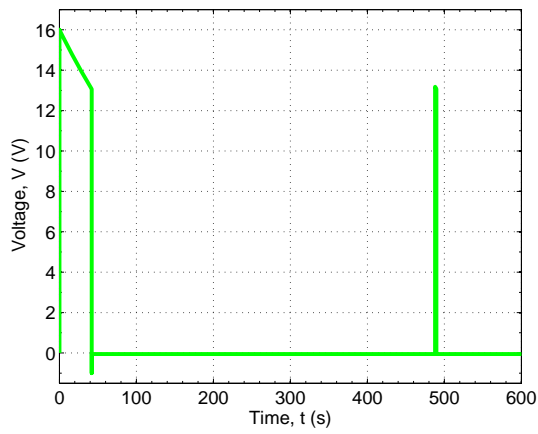
(b) Current through the free-wheeling MOSFETs



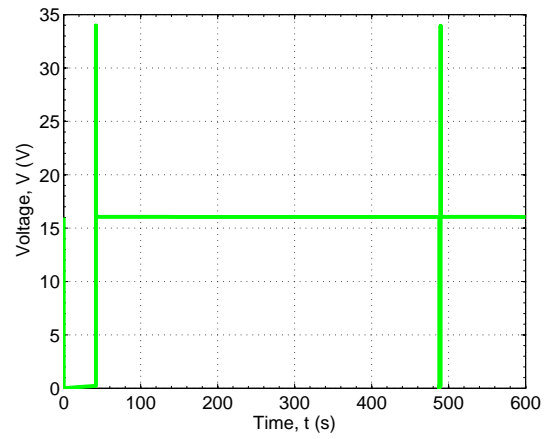
(c) Current through the discharge diodes



(d) Current through the HTS coil during discharge



(e) Voltage across the HTS coil



(f) Voltage across the low side MOSFET

Figure 7.13: The PLECS simulated results from the new circuit shown in Fig. 7.12.

Fig. 7.13(c) shows that the commutation series diodes did not turn-on during any of the simulated modes. Fig. 7.13(d) presents the discharge event by switching off the bottom MOSFET and letting the field current decay into the commutation diodes. These show that by splitting the control of the top and bottom MOSFETs, the circuit still behaves very similar to the original circuit with the exception of not turning on the commutation diodes. The voltage across the HTS coil is shown in Fig. 7.13(e). There was very little voltage undershoot across the coil significantly reducing any fast voltage transients across the back-to-back MOSFETs and series diodes. The voltage across the low-side MOSFET is shown in Fig. 7.13(f), the voltage overshoot during turn-off was limited to approximately 18 V (34 V total).

## 7.4 Cryogenic Setup of the HTS Coil

The HTS coil used in this demonstration model is made from the second generation high temperature superconducting (2G-HTS) wire, based on the YBCO material (manufactured by Zenenergy Power). Similar coils have been used in the world's first HTS hydro generator - the *HYDROGENIE project* power plant in Bavaria, Germany [109] [110]. The HTS coil is cooled by thermally sinking the coil to the cooling pipes with helium gas flowing through it at 30 K. The cryogenic setup of the HTS coil inside the high vacuum cryogenic enclosure is illustrated in Fig. 7.14, it shows the basic electrical and thermal conduction path. The in-flow current from the external power supply is thermally connected to the cooling clamp at the in flow helium gas pipe. This is to minimise any thermal leakage via the electrical connections into the HTS coil. A second cooling clamp is placed at the out flowing helium gas connection. By placing the power MOSFETs on the second cooling clamp, it is possible to chill the power MOSFETs down to cryogenic temperatures. Also, since the second cooling clamp is at the out flowing helium gas connection, all the thermal energy generated by the power MOSFETs can then be extracted to the chiller outside the enclosure.

The figure also illustrates the free-wheeling path between the power MOSFETs and the HTS coil. It is very important that the heat generated from the power MOSFETs does not

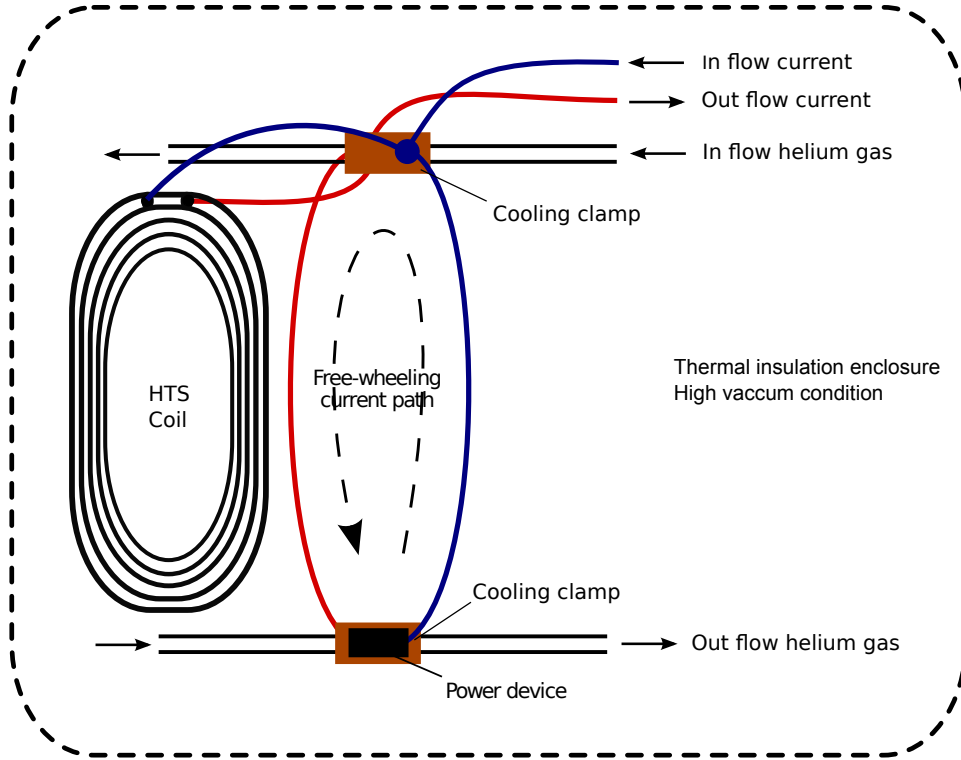


Figure 7.14: The cryogenic arrangement of the HTS coil within the thermal insulating enclosure.

flow back to the HTS coil, via the electrical connections. Sufficient heat flow into the HTS coil could induce quench events which must be avoided. However, the electrical wiring for the free-wheeling path should also be kept as short as possible to reduce any conduction losses in between.

## 7.5 Heatsink Design

The heatsink for the free-wheeling demonstration model was designed to cool the power devices by thermally sinking to the cooling clamp which is attached to the 30 K helium gas pipe. The heatsink also has to cool the free-wheeling current connections in order to minimise any heat flowing back towards the HTS coil. The design assumes no thermal convection will occur due to the high vacuum environment inside the cryo-chamber and thermal radiation is also assumed to be negligible. Therefore, only thermal conduction has been considered for

the heatsink design.

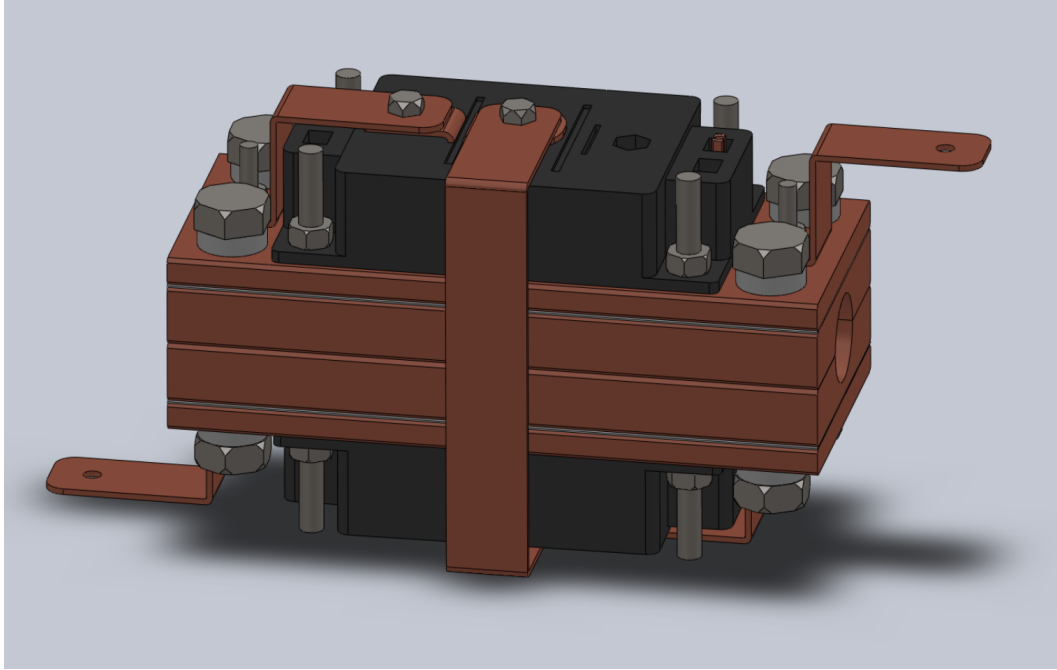


Figure 7.15: The heatsink design.

Fig. 7.15 presents a three dimensional sketch of the heatsink design in Solidworks. The figure illustrates all the components including the cooling clamp. The heatsink utilises both the top and bottom face of the cooling clamp in order to maximise the available space for thermal conduction. Almost all of the heat generated by the power MOSFET module will be transfer through the base plate into the copper plate directly attached underneath, which is thermally sinked to the cooling clamp (see appendix C for illustrations of the copper plates and cooling clamp). Heat leaked via the electrical terminals will be thermally sinked to the same copper plate before reaching the first cooling clamp at the in flow helium gas pipe. This will minimise the heat flow to the HTS coil.

The current path through the back-to-back MOSFETs and heatsink is illustrated in Fig. 7.16. The path is highlighted in blue and the direction of the current is illustrated by the arrows. The current first enters the copper terminal at the end of the copper plate, the current then flows through the copper plate beneath the module and out of the other side into the drain of the top MOSFET. The current then leaves the top MOSFET through the



source terminal (centre terminal of the module) and is conducted via a source to source copper lead at the side of the heatsink down to the bottom MOSFET. The current then flows through the bottom MOSFET and out of the drain terminal. The current then flows through the bottom copper plate and out of the other side, thermally sinking the electrical connections. The base plate of the power MOSFET module is electrically isolated from the dies inside the module and therefore does not electrically conduct any current.

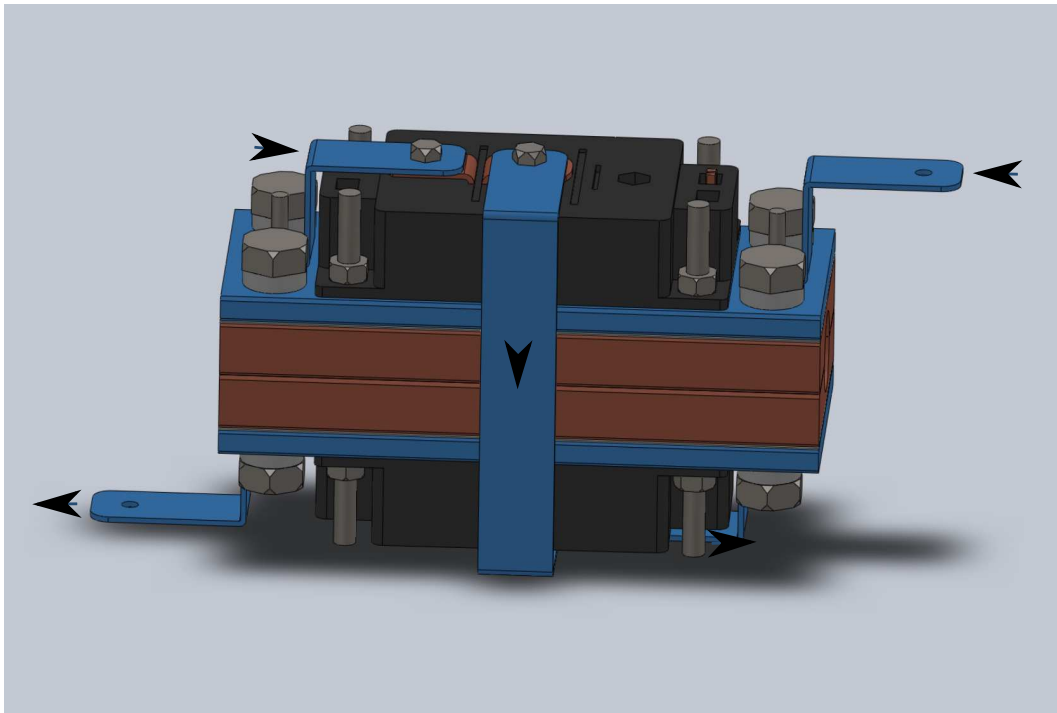


Figure 7.16: The current path (highlighted in blue) through the back-to-back MOSFETs and heatsink.

Fig. 7.17 illustrates how the heatsink is assembled. The heatsink is centred around the copper cooling clamp. Two copper plates are placed on either side of the cooling clamp with a 0.5 mm thick layer of G10 fibre glass in between for electrical isolation. The G10 fibre glass has to be thin to minimise the thermal resistance between the copper plate and the cooling clamp. Four M10 bolts are used to secure the copper plates to the cooling clamp, as well as to secure the cooling clamp to the helium gas pipe. Each M10 bolt is electrically isolated from the copper plate by two Nylon washer blocks. This is important

to stop current flowing between the top and bottom copper plates. Each copper plate has specifically located through-holes to secure the power MOSFET module using M5 bolts, as well as secure holes for the electrical connections. The source to source connection is secured by bolts on the source terminals and it is important to ensure the connection does not touch any of the copper plates or cooling clamps. This can be avoided by wrapping the source to source connection with insulating materials.

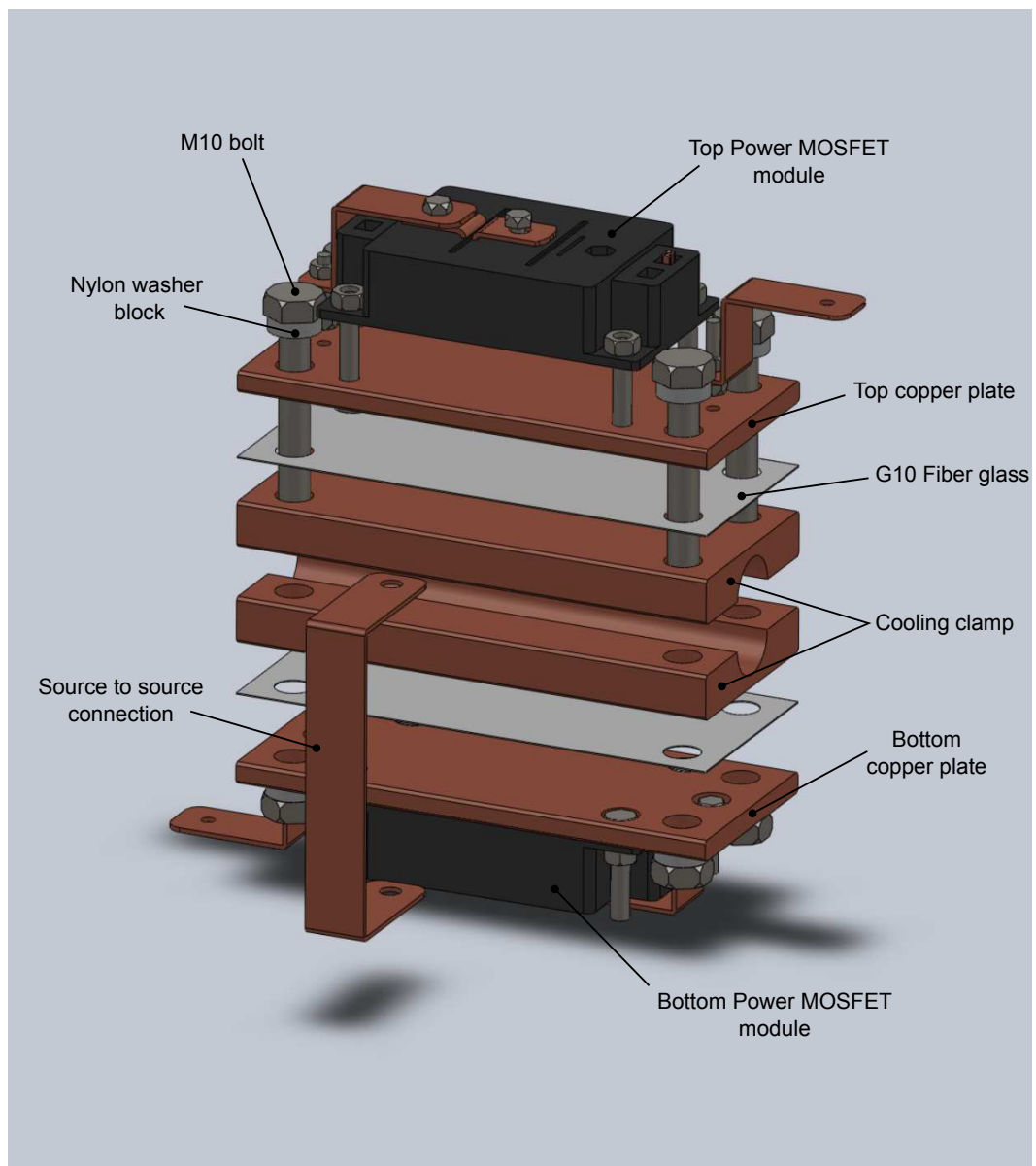


Figure 7.17: An exploded view of the heatsink assembly.

### 7.5.1 Thermal Simulation

The steady state thermal profile of the heatsink was simulated at 30 K, by using the thermal analysis function in Solidworks, the simulation assumes a constant heat source and constant thermal conduction at the helium gas pipe. No convection or thermal radiation was included in the simulation.

Using the on-state resistance measurements in section 7.2 and assuming identical dies were used in the (IXTK 140N20P) TO-264 packaged devices and the power MOSFET modules (VMO 1600-02P), the on-state resistance for the power MOSFET module were extrapolated at 30 K. The calculated power loss at 130 A was assumed to be  $\sim 3.5$  W per MOSFET module, a total of 7 W power loss. The majority of heat generated was assumed to conduct from the baseplate of the power module into the copper plate attached (The base plate is shown on the right figure (bottom view) of Fig. 7.18). All of the copper based components in the heatsink were assumed to be made from oxide-free high conductivity (OFHC) copper which has a known thermal conductivity of  $2140 \text{ W/mK}$  at 30 K. The G-10 fibre glass sandwiched between the copper plate and cooling clamp has a thermal conductivity of  $0.2256 \text{ W/mK}$  at 30 K and a specific heat capacity of  $1386 \text{ J/kg K}$ .

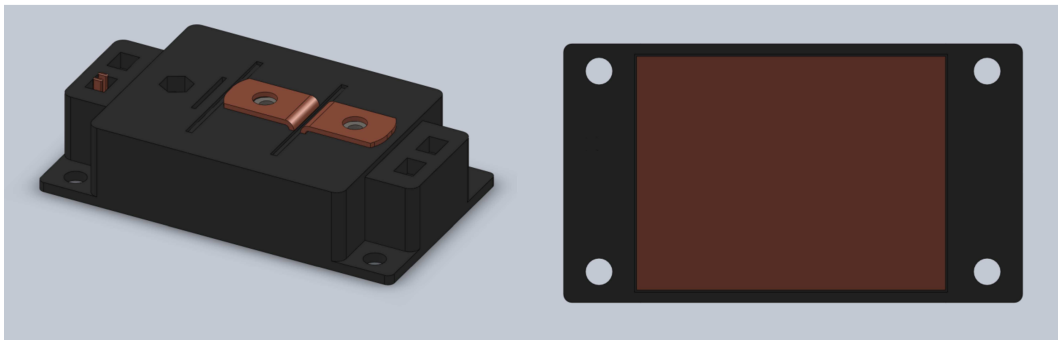


Figure 7.18: The isometric view of the power MOSFET module (VMO 1600-02P) on the left and bottom view on the right.

The results of the simulated steady state heatsink temperature are presented in Fig. 7.19. The results are presented in a range of colours, indicating difference in temperatures, with the deepest shade of blue being at 30 K and bright red at 31 K. The highest simulated temperature is at the body of the module and it is  $<0.5$  K above 30 K. The temperatures

at the indicated location points in the figure are presented in Table. 7.1. Point A is the temperature of the electrical connection to the first cooling clamp at the in flow gas pipe, the simulated temperature is only 0.16 K above the gas line temperature. This shows the heatsink design is adequate for this application.

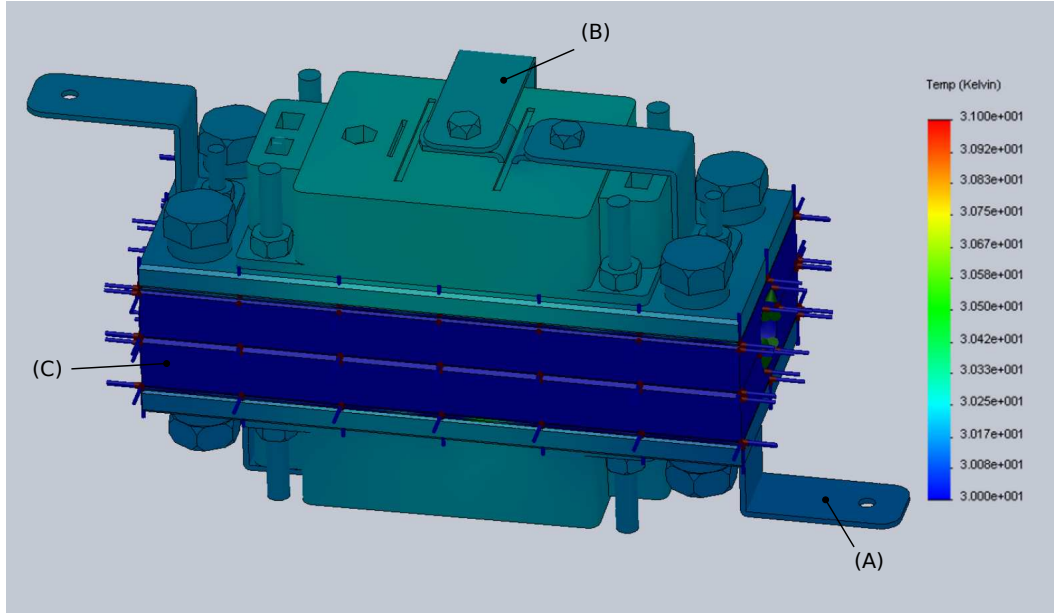


Figure 7.19: The simulated steady state heatsink temperature.

Table 7.1: Temperature probed at the points located in Fig. 7.19

Points	Temperature
A	30.16 K
B	30.23 K
C	30 K

## 7.6 Conclusion

This chapter describes the design of the free-wheeling demonstration circuit. From the analysis and simulation of back-to-back MOSFETs configuration to the control sequence of

the circuit. Reasons were given for the selection of the power device, the PolarHT Module, as well as the modifications of the device packaging for cryogenic operations. The setup of the cryogenic circuit was also introduced and the thermal heatsink design was described and analysed.

## 8.1 Conclusions

With the global surging demands for renewable energy, wind power technology stands to be in a good position for growth. The current trend in wind turbine design is the use of HTS wires to form the high power magnetic components. Converteam (now part of GE Energy) is a technology leader in HTS motors and generators. They want to incorporate power devices into the cryogenic parts of wind turbine systems, but are uncertain about the validity of the idea since commercially available power devices are only rated down to  $-40\text{ }^{\circ}\text{C}$ . This study is an industrial orientated investigation into the cryogenic behaviour of power devices for the the next generation of HTS wind turbines. The core aim is to identify which power devices can be used and demonstrate their cryogenic operation.

Within the large selection of commercially available power devices, Si power MOSFETs were found to be the best likely candidate through analysing their known behaviour in the literature review in chapter 2. This is due to a number of factors: the unique requirements of the intended applications, the weakness of the forward threshold voltages in most bipolar devices, the large reduction in on-state resistance, the ease of control of power MOSFETs, as well as the possible room for optimisations for cryogenic operation. Below is a list of the core findings from this work, based on the cryogenic characterisation of power devices and

analysis into their measured behaviour down to 20 K:

- In most cases between identical power MOSFETs, large variation in the on-state resistance have been observed below 50 K. Some exhibited large degradation from 50 K down to 20 K, some exhibited no degradation over the same temperature range.
- Through theoretical analysis, it has been proposed that the reason behind the large variation in on-state resistance is due to the sensitivity of the free carrier concentration to the background doping concentration of the JFET region near the surface of the oxide interface. This is the likely factor that controls the initial free carrier concentration at low voltage conditions at temperatures below 50 K.
- This large variation of the on-state resistance could be mitigated by careful control of the background doping concentration at the JFET region.
- The drift region of super-junction device could be further optimised for operation below 50 K to achieve better breakdown voltages and on-state resistances .
- In contrary to the predicted linear degradation of breakdown voltages down to 77 K, commonly seen in previous literatures, it has been found that the degradation levels-off at temperature below approximately 100 K. The gradient of the breakdown voltage with decreasing temperature is dependent on the dopant concentration of the drift region as well as the device structure type.
- Measured data have demonstrated that SiC MOSFET can operate at cryogenic temperatures but unlike Si power MOSFET, it exhibited no improvements when operating at lower temperatures. This is likely due to the degradation of the channel mobility at low temperature as well as the stronger carrier freeze-out effect in SiC materials.
- Measured data have shown that GaN HEMT exhibits no carrier freeze-out effect, which supports the theoretical idea of the temperature independence of the free carrier concentration at the channel.

With the aim to demonstrate the applicability of power MOSFETs within the intended free-wheeling application, a demonstration circuit was designed and built. A back-to-back MOSFETs configuration was proposed and simulated using the circuit simulation PLECS software. A split gate control of the top and bottom MOSFETs were found to be the best solution to avoid fast voltage transients. The IXYS PolarHT™ Module was selected for the demonstration model due to their measured low average on-state resistance at temperatures below 50 K. In order to ensure good cryogenic operation for the power module, the silicone gel was removed to avoid crystallisation at low temperatures. To avoid thermal leakage to the HTS coil during operating, a heatsink with the capability to sink heat from the electrical connections was also designed, simulated and built.

## 8.2 Further Work

### 8.2.1 Operating Temperatures Below 20 K

The lowest measured temperature of this work is 20 K. This is due to the limited achievable temperature of the cryogenic rig. Furthermore, the required operating temperature of the intended free-wheeling application is 30 K, which means in this case it is not necessary reach lower temperatures. However, there are applications that could require device operation below 20 K, down to 4 K or even lower. The most famous example is the large hadron collider (LHC) in between the French and Swiss border [111]. The cryogenic behaviour of some power MOSFETs [26] and even IGBTs [42] have been measured down to 4 K. Both studies have shown serious degradation in the performance of power devices at 4 K. However, their behaviour were not fully understood and therefore further investigation would be required.

For silicon based power MOSFET, operating at temperatures below 20 K would further enhance the carrier freeze-out effect. At the liquid helium temperature of 4 K, even the electric field dependent Poole-Frenkel ionisation (see chapter 3.2) would struggle to operate effectively since it is still fundamentally a thermal excitation process. Therefore, silicon power MOSFETs would have a limit to the lowest operating temperature which could still



result in an improvement when compared to room temperature operations. A better solution would be to look for a device whose carrier concentration in the conduction path is not or at least weakly dependent on temperature. In this study, GaN HEMT devices have been shown to exhibit no carrier freeze-out behaviour down to 20 K, further investigations could measure similar devices down to 4 K or lower to investigate their behaviour.

### 8.2.2 High Voltage Blocking

In high voltage applications, bipolar devices such as IGBT/thyristors are generally used, however the on-state losses will be limited by the forward threshold knee voltage and carrier freeze-out effect. This is especially important when operating at cryogenic temperatures where on-state losses must be kept at a minimum. Following this logic, paralleling power MOSFETs could potentially achieve lower on-state losses. The normalised on-state resistance against number of MOSFET devices in parallel is shown in Fig. 8.1.

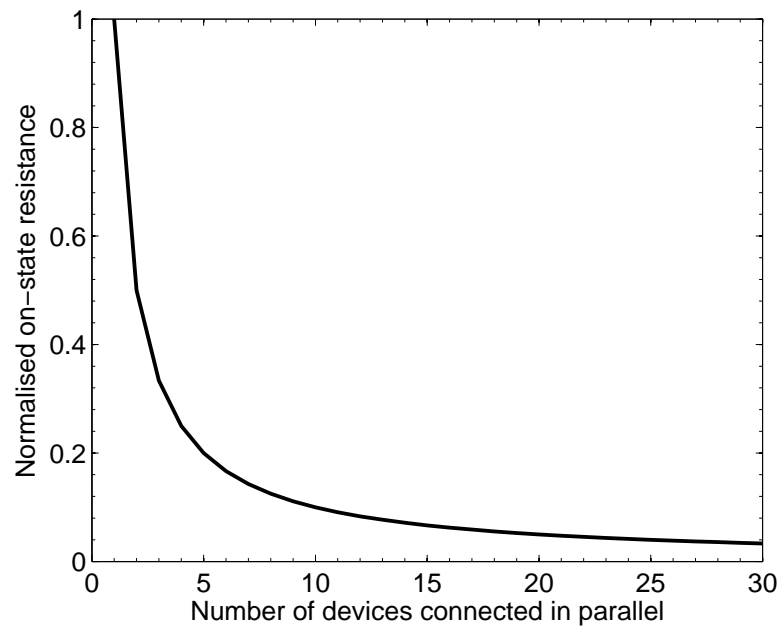


Figure 8.1: Normalised on-state resistance against number of power MOSFETs connected in parallel.

For power devices, the degradation of breakdown voltage at cryogenic temperature is

unavoidable. Chapter 5 has shown that from room temperature down to 20 K, breakdown voltages decrease between 25 to 33 % (depending on the device type and voltage ratings). For Si power MOSFET, the highest rated blocking voltage that is commercially available is 1500 V and this should reduce down to approximately 1000 V at 20 K. which means the achievable breakdown voltage from a single power MOSFET is limited to 1000 V at 20 K. The on-state resistance of this device has been shown to be very poor. Even after paralleling five devices to achieve current rating of 20 A, the on-state resistance is still at 3  $\Omega$  at 20 K. A better option would be to stack three 500 V HEXFETs (20 A rated) in series, this should achieve a breakdown voltage of approximately 1200 V and an on-state resistance of approximately 90 m $\Omega$ . Giving a 33 times lower on-state resistance when compared to the five paralleled 1500 V power MOSFETs. However, this would not be a cost effective option and the control of many stacked power MOSFET would be complex.

Non Si devices such as SiC MOSFETs and GaN HEMTs should also be considered since they can naturally sustain higher breakdown voltages. Data on SiC Schottky diodes in chapter 5.3 indicate that the breakdown voltage degradation from room temperature down to 20 K can be as low as 10 %. However, data on SiC MOSFET also indicate increased on-state resistance with decreasing temperature, which would eliminate the advantage of operating devices at cryogenic temperatures. Data on the GaN HEMT indicated breakdown voltage degradation of approximately 34 % over the same temperature range. However, GaN HEMT technology is still relatively new and immature. Further work is required when the technology matures.

### 8.2.3 Reliability

In general, operating devices at lower temperatures will improve reliability and operational lifetime due to the reduced degradation from heating elements. Within all the measured power devices in this work, none has fail due to operating at cryogenic temperatures. However, the selected devices were only limited to small device packages such as TO-220 and TO-247. This was due to the size of the cold-head, which could only accommodate small device packages. Furthermore, all the device characteristics measured by the high power

curve tracer was performed using short pulses ( $250\ \mu\text{s}$ ) of voltages. This is to reduce the self heating effect of the device to obtain the actual device behaviour. However, this is not be a realistic approach to understand reliability of the device during realistic operations. Chapter 7 aimed to address this issue by operating the devices in realistic operation. Nevertheless, further work is required to assess the long term reliability of these devices, such as quantifying failure rates. Power/thermal cycling should also be performed to understand the effects they have on the semiconductor device, packaging and interconnects at cryogenic temperatures.

Degradation effects due to cryogenic operations must be identified. These include semiconductor level effects such as long term degradation from high field transport mechanisms, degradation of the gate oxide and radiation effects, as well as packaging level issues such as difference in CTE between the materials inside the package and degradation of silicone gel. One improvement for the packaging of power modules is to use silicone gel-less module, as discussed in chapter 7.2.

### 8.2.4 Back-to-back Power MOSFET Module Optimisation

Within commercially available power devices, two power MOSFETs in the back-to-back configuration has been suggested in this study as the best solution for the requirements introduced in chapter 1.2. The current design presented in chapter 7 involve two individual power MOSFET modules connected externally. This can be further optimised to improve performance of the configuration, below is a list of optimisations that has been considered:

- Single module design - Two individual MOSFETs can be integrated into a single power module with the configuration shown in Fig. 8.2(a). This will reduce the interconnect resistances between individual modules and reduce the stray inductance at the source terminal. Furthermore, the single module becomes a stand alone and space saving solution.
- Single die design - The back-to-back configuration can be integrated into a single die. Fig. 8.2(b) present an illustration of the basic device structure of this arrangement.

This solution could reduce the number of bond wires required and therefore further reduce the on-state resistance and improve reliability. In addition, this compact design can be optimised to improve the spacing inside the module in order to increase power density. However, the device would require good electrical isolation between the back-to-back MOSFETs. Furthermore, isolation methods such as deep trench isolation are relative expensive and difficult to achieve trenches all the way through the die.

- Build in thermal sink - The thermal sink of the drain connections can be integrated into the module design. The simplest solution would be to use copper tracks on top of the direct copper bond substrate in order to sink the heat.

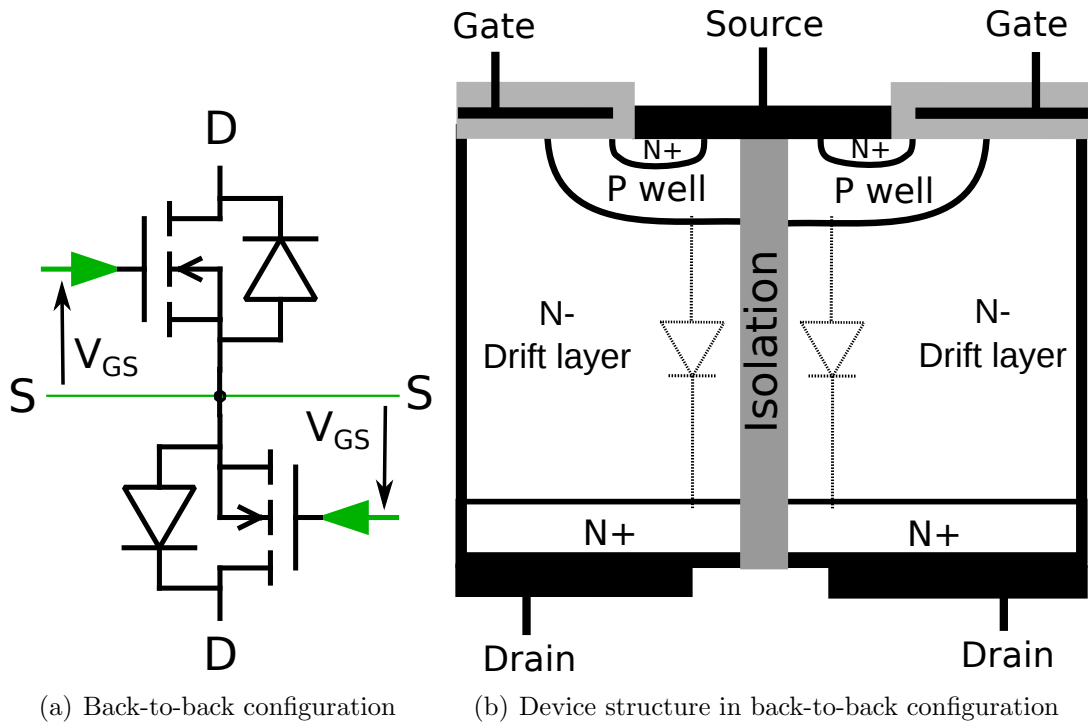


Figure 8.2: Illustrations of two power MOSFETs in (a) back-to-back circuit configuration and (b) back-to-back configuration within a single die structure.

### 8.2.5 Cryogenic Free-wheeling Test

The cryogenic free-wheeling test was intended to be performed with the HTS coil at Converteam UK, in Rugby. Unfortunately, due to various technical problems with the HTS coil, the test could not be performed within the allocated time period. Therefore, experimental data cannot be obtained to verify the simulation work presented in this thesis at the time of submission. Converteam intends to perform the cryogenic test once the HTS coil is available.

### 8.2.6 Other Applications

This work which has been to analyse commercially available power devices for the purpose of applying it into the next generation of HTS wind turbines can also be applied in other similar applications. The benefits of lower on-state resistance is universal and the result is almost always higher system efficiency. The knowledge gained in this study can be transferred to any other electrical application with existing cryogenic system or environment that requires some form of control of DC current, such as HTS motors, generators, magnetic resonance imaging (MRI) machines and deep space exploration. Furthermore, this study can be extended to applications such as synchronous rectification at cryogenic temperatures.

1. Kenneth Leong, Angus Bryant, Philip Mawby, “Status & Trends of Devices Technology for Cryogenic Power Electronics”, *9<sup>th</sup> International Seminar on Power Semiconductors*, 2008.
2. Kenneth Leong, Angus Bryant, Philip Mawby, “The Cryogenic behaviour of High Power Si and GaAs Schottky ”, *International Conference on Solid State Devices and Materials*, 2009.
3. Kenneth Leong, Angus Bryant, Philip Mawby, “Power MOSFET Operation at Cryogenic Temperatures: Comparison between HEXFET® , MDMesh™ and CoolMOS™”, *22<sup>nd</sup> International Symposium on Power Semiconductor Devices and ICs*, 2010.
4. Kenneth Leong, Angus Bryant, Philip Mawby, “Super-junction MOSFET Optimisation for Ultra Low (< 50K) Temperature Operation”, *10<sup>th</sup> International Seminar on Power Semiconductors*, 2010.
5. Kenneth Leong, Benedict Donnellan, Angus Bryant, Philip Mawby, “An Investigation into the Utilisation of Power MOSFETs at Cryogenic Temperatures to Achieve Ultra-low Power Losses”, *IEEE Energy Conversion Congress & Exposition*, 2010.

Information on the selected PolarHT power MOSFET module (VMO1600-02P) is presented in this section. Fig. B.1 shows the epoxy layer inside the power module after removing the plastic encasing. The epoxy layer was found to be approximately 4 mm in thickness. Fig. B.2 shows the exposed dies inside the power module after milling two holes through the epoxy layer and removing the silicone gel with silicone de-polymeriser solution. Fig. B.3 - B.8 shows the datasheet of the PolarHT power MOSFET module.



Figure B.1: Opened PolarHT power MOSFET module (VMO1600-02P) showing the epoxy layer.

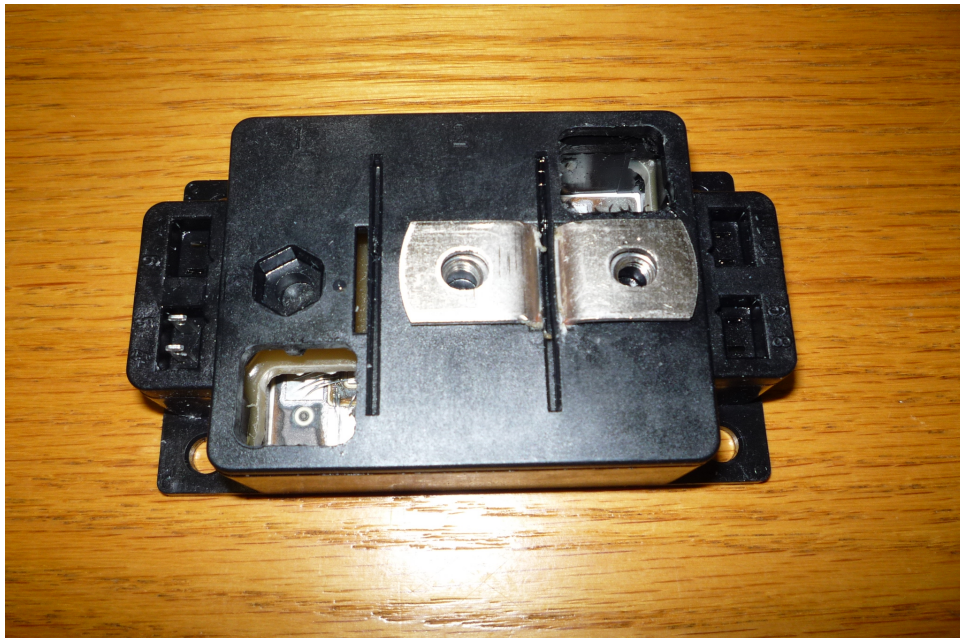


Figure B.2: Opened PolarHT power MOSFET module (VMO1600-02P) after silicone gel removal.

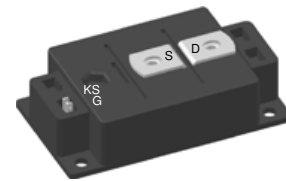
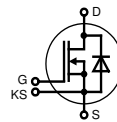


## PolarHT™ Module

N-Channel Enhancement Mode

$$\begin{aligned} V_{DSS} &= 200 \text{ V} \\ I_{D80} &= 1600 \text{ A} \\ R_{DS(on)} &= 1.7 \text{ m}\Omega \text{ max.} \end{aligned}$$

Preliminary data



MOSFET				
Symbol	Conditions	Maximum Ratings		
V <sub>DSS</sub>	T <sub>VJ</sub> = 25 °C to 150 °C	200	V	
V <sub>GS</sub>		± 20	V	
I <sub>D25</sub>	T <sub>C</sub> = 25 °C	1900	A	
I <sub>D80</sub>	T <sub>C</sub> = 80 °C	1600	A	
I <sub>F25</sub>	T <sub>C</sub> = 25 °C (diode)	1900	A	
I <sub>F80</sub>	T <sub>C</sub> = 80 °C (diode)	1600	A	
Symbol	Conditions	Characteristic Values		
(T <sub>VJ</sub> = 25 °C, unless otherwise specified)				
		min.	typ.	max.
R <sub>DSon</sub>	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 1600 A; T <sub>VJ</sub> = 25 °C T <sub>VJ</sub> = 125 °C		1.58 3.25	1.7 3.6
				mΩ mΩ
V <sub>GS(th)</sub>	V <sub>DS</sub> = 20 V; I <sub>D</sub> = 5 mA	2.5		5
				V
I <sub>DSS</sub>	V <sub>DS</sub> = V <sub>DSS</sub> ; V <sub>GS</sub> = 0 V; T <sub>VJ</sub> = 25 °C T <sub>VJ</sub> = 125 °C		5.0	0.5
				mA mA
I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V; V <sub>DS</sub> = 0 V			2
				μA
Q <sub>g</sub>	V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0.5 · V <sub>DSS</sub> ; I <sub>D</sub> = I <sub>D80</sub>		2900	
Q <sub>gs</sub>			600	
Q <sub>gd</sub>			1600	
				nC nC nC
t <sub>d(on)</sub>	inductive load V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 100 V I <sub>D</sub> = 1600 A; R <sub>G</sub> = 1.8 T T <sub>VJ</sub> = 25 °C		320	
t <sub>r</sub>			1220	
t <sub>d(off)</sub>			620	
t <sub>f</sub>			700	
E <sub>on</sub>			24	
E <sub>off</sub>			152	
E <sub>rec</sub>			3.7	
				mJ mJ mJ
t <sub>d(on)</sub>	inductive load V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 100 V I <sub>D</sub> = 1600 A; R <sub>G</sub> = 1.8 T T <sub>VJ</sub> = 125 °C		340	
t <sub>r</sub>			1220	
t <sub>d(off)</sub>			740	
t <sub>f</sub>			580	
E <sub>on</sub>			28	
E <sub>off</sub>			147	
E <sub>rec</sub>			4.9	
				ns ns ns ns mJ mJ mJ
R <sub>thJC</sub>	with heat transfer paste		0.03	
R <sub>thJS</sub>				
				K/W

### Features

- PolarHT™ technology
  - low  $R_{DS(on)}$
  - dv/dt ruggedness
  - fast intrinsic reverse diode
- Package
  - low inductive current path
  - screw connection to high current main terminals
  - use of non interchangeable connectors for auxiliary terminals possible
  - Kelvin source terminals for easy drive
  - isolated ceramic base plate

### Applications

- converters with high power density for
  - main & aux. AC drives of electric vehicles
  - DC drives
  - power supplies

IXYS reserves the right to change limits, test conditions and dimensions.

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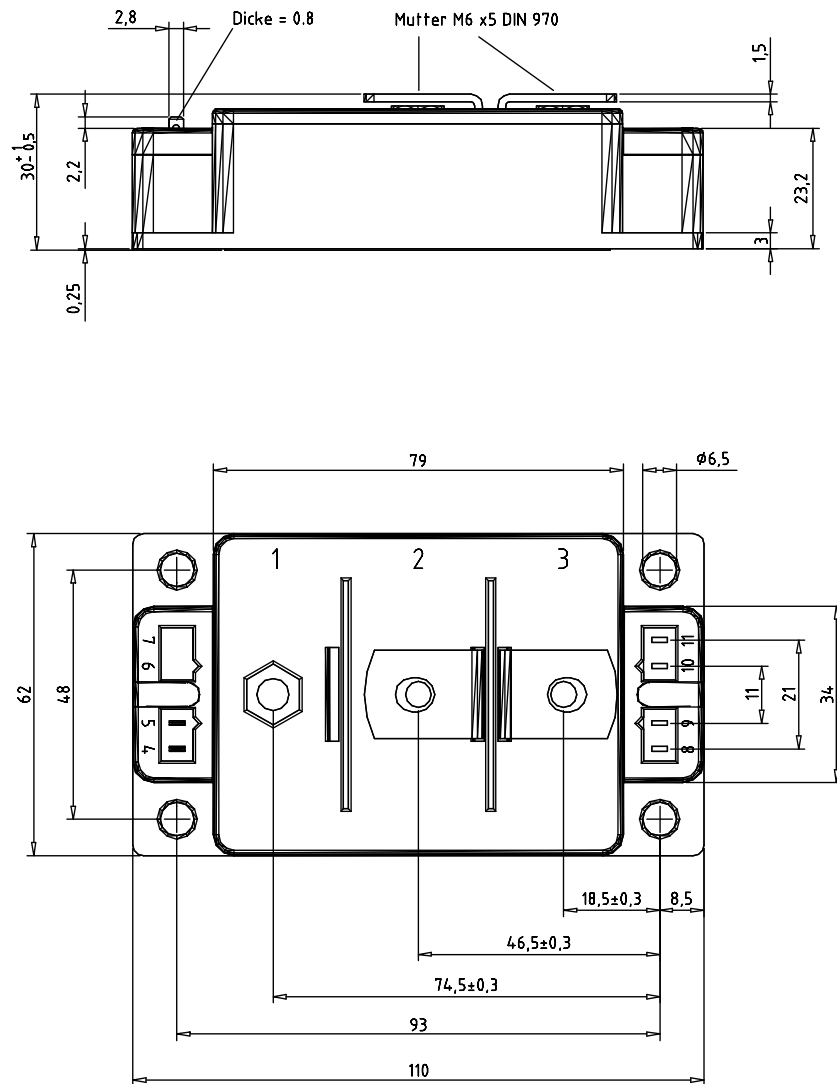
1 - 6

Figure B.3: PolarHT power MOSFET module (VMO1600-02P) datasheet, pg.1.

Source Drain Diode						
Symbol	Conditions	Characteristic Values				
		min.	typ.	max.		
$V_{SD}$	$I_F = 1600 \text{ A}; V_{GS} = 0 \text{ V};$ $T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$		1.17 1.13		V V	
$t_{rr}$ $Q_{rr}$ $I_{RM}$	$V_{DS} = 100 \text{ V}; I_F = 1600 \text{ A}$ $dV_F/dt = 1300 \text{ A}/\mu\text{s}$ $T_{VJ} = 25^\circ\text{C}$		340 40 210		ns $\mu\text{C}$ A	
$t_{rr}$ $Q_{rr}$ $I_{RM}$	$V_{DS} = 100 \text{ V}; I_F = 1600 \text{ A}$ $dV_F/dt = 1300 \text{ A}/\mu\text{s}$ $T_{VJ} = 125^\circ\text{C}$		380 56 250		ns $\mu\text{C}$ A	

Module						
Symbol	Conditions	Maximum Ratings				
$T_{VJ}$ $T_{slg}$			-40...+150 -40...+125		$^\circ\text{C}$ $^\circ\text{C}$	
$V_{ISOL}$	$I_{ISOL} \leq 1 \text{ mA}; 50/60 \text{ Hz}$		3600		V~	
$M_d$	mounting torque (M6) terminal connection torque (M6)		2.25 - 2.75 4.5 - 5.5		Nm Nm	
Symbol	Conditions	Characteristic Values				
		min.	typ.	max.		
Weight			250		g	

Ordering	Part Name	Marking on Product	Delivering Mode	Base Qty	Code Key
Standard	VMM 1600-02P	VMM 1600-02P	Box	2	



**Optional accessories for modules**

**Dimensions in mm (1 mm = 0.0394")**

keyed twin plugs  
(UL758, style 1385, CSA class 5851,  
guide 460-1-1)

- Type ZY180L with wire length 350 mm  
for pins 4 (Gate, yellow wire)  
and 5 (Kelvin Source, red wire)

Figure B.5: PolarHT power MOSFET module (VMO1600-02P) datasheet, pg.3.

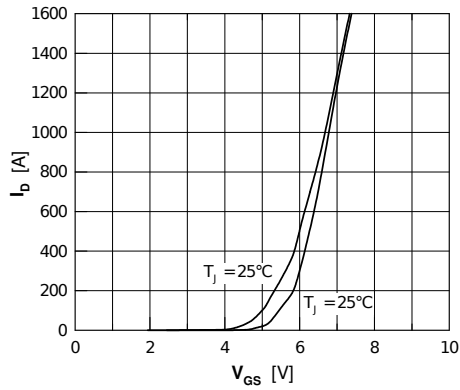


Fig. 1 Typical transfer characteristic

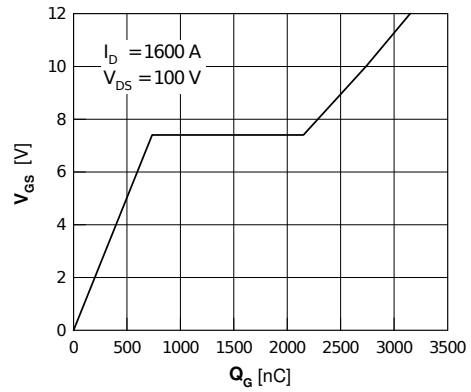


Fig. 2 Typical gate charge characteristic

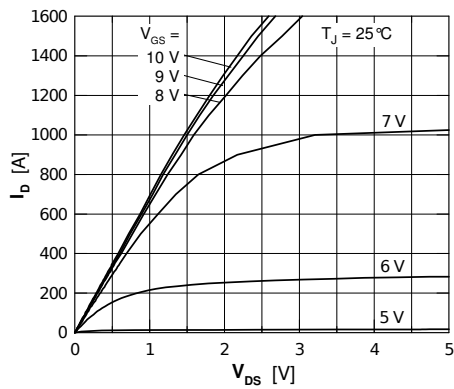


Fig. 3 Typical output characteristic

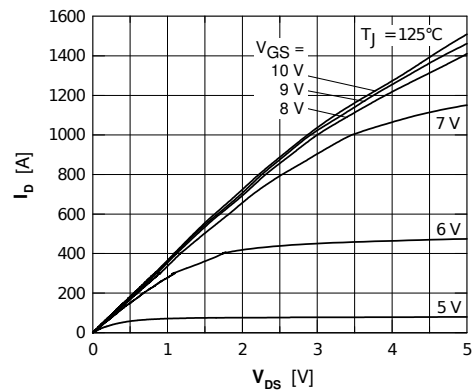


Fig. 4 Typical output characteristic

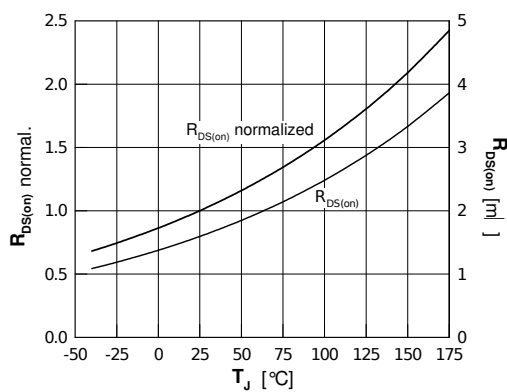


Fig. 5 Typ. drain source on-state resistance  $R_{DS(on)}$  versus junction temperature  $T_{J}$

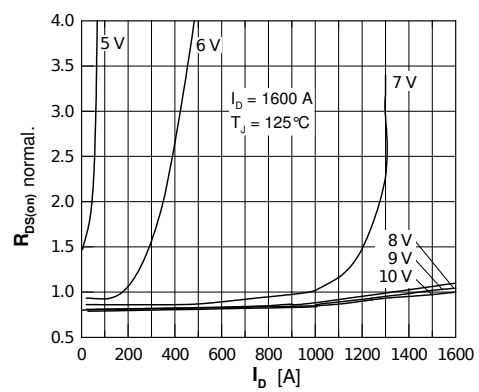


Fig. 6 Typ. drain source on-state resistance  $R_{DS(on)}$  versus  $I_D$

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Figure B.6: PolarHT power MOSFET module (VMO1600-02P) datasheet, pg.4.

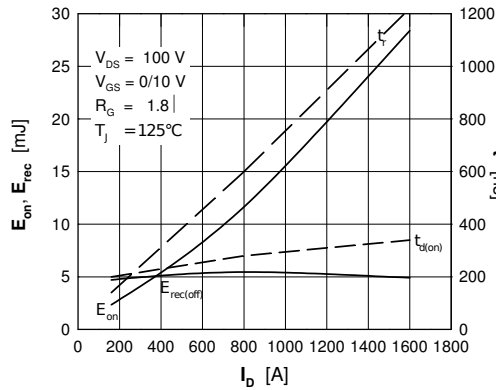


Fig. 7 Typ. turn-on energy & switching times vs. drain source current, inductive switching

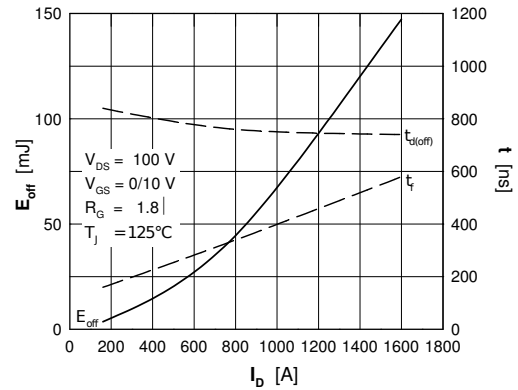


Fig. 8 Typ. turn-off energy & switching times vs. drain source current, inductive switching

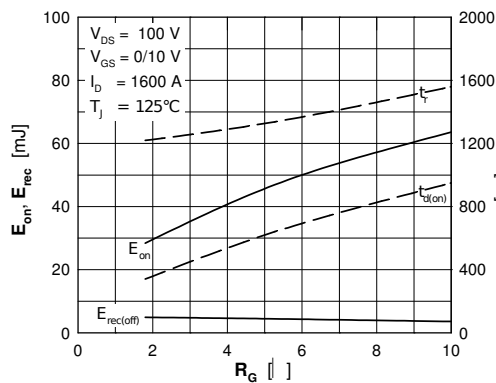


Fig. 9 Typ. turn-on energy & switching times vs. gate resistor, inductive switching

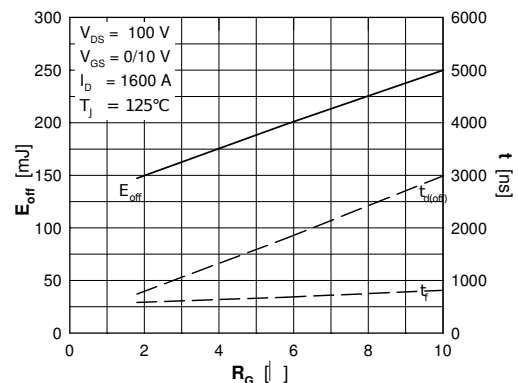


Fig. 10 Typ. turn-off energy & switching times vs. gate resistor, inductive switching

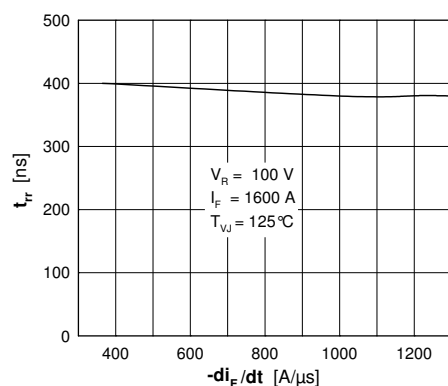


Fig. 11 Typ. reverse recovery time  $t_{rr}$  of the body diode versus  $di/dt$

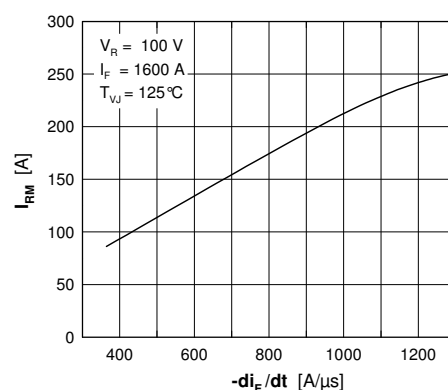


Fig. 12 Typ. reverse recovery current  $I_{RM}$  of the body diode versus  $di/dt$

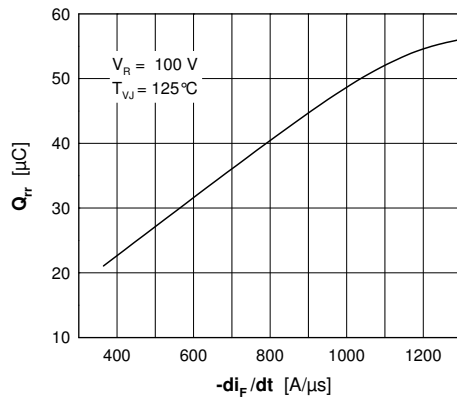


Fig. 13 Typical reverse recovery charge  $Q_{rr}$  of the body diode versus  $di/dt$

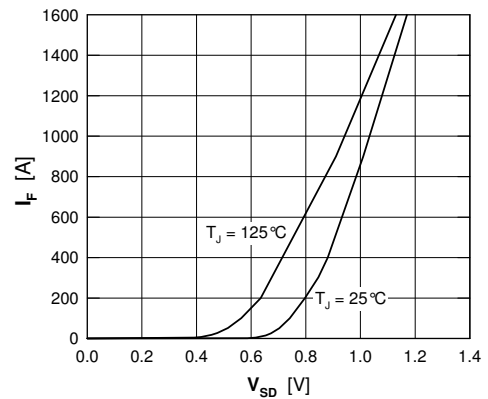


Fig. 14 Source drain current  $I_F$  (body diode) vs. typical source drain voltage  $V_{SD}$

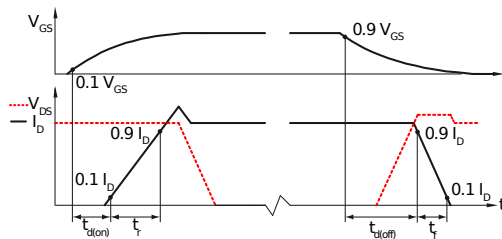


Fig. 15 Definition of switching times

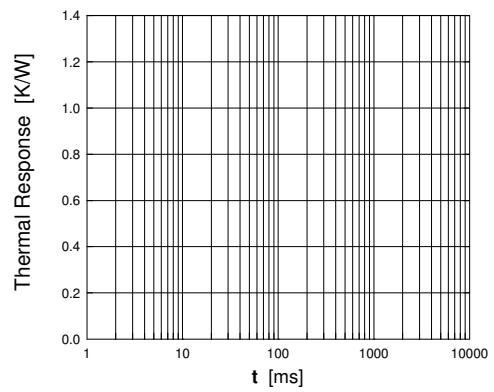


Fig. 16 Typ. thermal impedance junction to heatsink  $Z_{thJH}$  with heat transfer paste

Fig. C.1 shows the two copper plates on the left side, the cooling clamp on the right side.

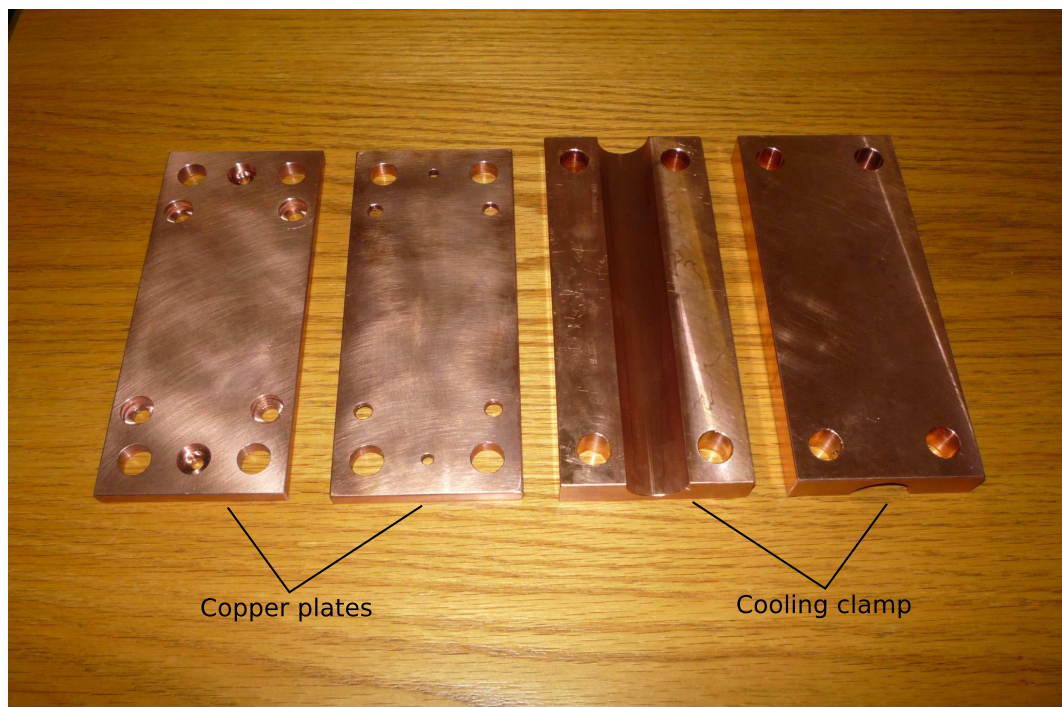


Figure C.1: The two copper plates and cooling clamp.

# D Cryogenic System

Fig. D.1 shows the modified switch box connection to the high power curve tracer (Tektronix® 371B). The switch box enable forward and reverse characteristic of the power devices without physically rewiring connections during measurements. Fig. D.3 shows the coldhead of the cryogenic rig. Fig. D.2 shows part of the cryogenic rig showing the cryostat chamber, the temperature controller and rotary vacuum pump.



Figure D.1: Modified switch box connection to the high power curve tracer (Tektronix® 371B).





Figure D.2: The cryogenic rig - showing the cryostat chamber, the temperature controller and rotary vacuum pump.



Figure D.3: The coldhead of the cryogenic rig.

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